

NuMicro™ Series NM1510/520/530 Preliminary Data Sheet

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1 GENERAL DESCRIPTION

The NuMicro™ NM15xx Series 32-bit microcontroller is embedded with the newest ARM® Cortex™-M0 core at a cost equivalent to traditional 8-bit microcontroller for industrial control and applications which need high performance.

The NuMicro™ NM15xx Series embedded with the Cortex™-M0 core runs up to 72 MHz and supports a variety of industrial control and applications which need high CPU performance. The NuMicro™ NM15xx Series provides 128K/64K/32K bytes embedded flash, 4 Kbytes data flash, 4 Kbytes flash for the ISP, and 16K/8K/4K/2K bytes embedded SRAM. This MCU includes advanced PWM function, MDU (motor drive unit) and input capture timer which are specially designed for motor driving application. It is also equipped with plenty of peripheral devices, such as Timers, Watchdog Timer, UART, SPI, I2C, PWM Timer, GPIO, 12-bit ADC, Low Voltage Detector and Brown-out detector. These useful functions make the NuMicro™ NM15xx Series powerful for a wide range of applications.

In addition, the NuMicro™ NM15xx Series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow user to update the program memory without removing the chip from the actual end product.

2 FEATURES

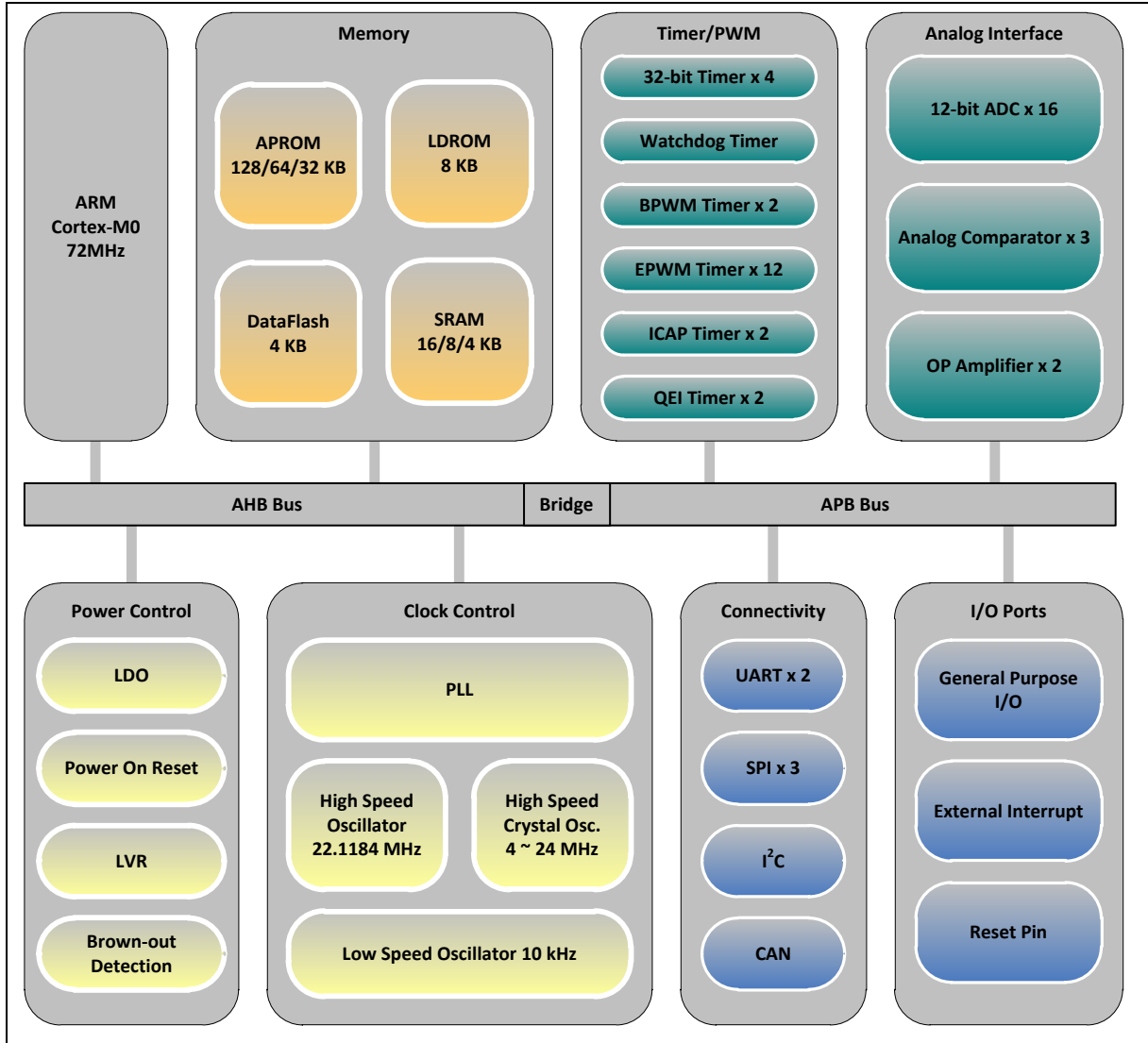
- Core
 - ARM® Cortex™ -M0 core runs up to 72 MHz
 - One 24-bit system timer
 - Supports low power sleep-mode
 - Single-cycle 32-bit hardware multiplier
 - NVIC for the 32 interrupt inputs, each with 4-levels of priority
 - Supports Serial Wire Debug (SWD) support with two watchpoints and four breakpoints
- Memory
 - 128K/64K/32K bytes Flash for program memory (APROM)
 - 8 Kbytes Flash memory for ISP loader (LDROM)
 - 4 Kbytes Flash memory for Data Flash
 - Supports In-system program (ISP) and In-application program (IAP) application code update
 - 16K/8K/4K bytes SRAM for internal scratch-pad RAM
 - Supports 2 wire ICP update from ICE interface
 - Supports fast parallel programming mode by external programmer
- Clock Control
 - Programmable system clock source
 - Built-in internal 22.1184 MHz OSC (trimmed to 1%) for system operation
 - Built-in low power 10 kHz OSC for watchdog timer and wake-up in sleep mode
 - External 4~24 MHz crystal input
 - Supports one PLL, up to 72 MHz, for high performance system operation
- Hardware divider
 - Supports signed 32-bit dividend, 16-bit divisor operation
- GPIO port
 - Up to 8-bit, 11-port I/O
 - Bit control available
 - Four I/O modes:
 - ◆ Quasi bi-directional
 - ◆ Push-pull (output with high driver and sink current)
 - ◆ Open-drain
 - ◆ Input only with high impedance (default)
 - TTL/Schmitt trigger input selectable
 - I/O pins configurable as interrupt source with edge/level setting
 - INT0 and INT1 pins with individual interrupt vectors

- Timers
 - Supports four channel 32-bit timers; one 8-bit pre-scale counter with 24-bit up-timer for each timer
 - 24-bit timer value is readable through TDR (Timer Data Register)
 - Supports One-shot, Periodic and Toggle operation modes
 - Supports event counter function
- Watchdog Timer
 - ON/OFF by hardware configuration or software
 - Multiple clock sources
 - Supports wake-up from Power-down or Sleep mode
 - Interrupt or reset selectable on watchdog time-out
 - Time-out reset delay period time can be selected
- WWDT (Window Watchdog Timer)
 - 6-bit down counter with 11-bit pre-scale for wide range window selected
- Basic PWM
 - 1 unit of 16-bit basic PWM, up to 2ch output
 - Alternative function as input capture timer
- Enhanced PWM
 - 2 units of 16-bit enhanced PWM, up to 6ch output with dead-zone control, brake and polarity control for motor drive
 - Default tri-state during any reset
- Enhanced Input Capture
 - Up to 2 units of 24-bit input capture
 - Each unit has 3 inputs: IC0, IC1 and IC2
- QEI (Quadrature Encoder Interface)
 - Up to 2 units of Quadrature Encoder Interface
 - Each unit has 3 inputs: QEIA, QEIB and IDX
- MDU (Motor Drive Unit)
 - Built-in PI + FOC + SVPWM
 - Output Space Vector PWM timing to PWM unit 0/1
- UART
 - Up to two 16550 compatible UART devices
 - Programmable baud-rate generator
 - Buffered receiving and transmitting, each with 16 bytes FIFO
 - Supports flow control (TX, RX, CTS and RTS)
 - Supports IrDA(SIR) function
 - Supports RS-485
- SPI
 - Up to three sets of SPI device
 - Supports SPI master/slave mode

- Full duplex synchronous serial data transfer
- Variable length of transfer data from 8 to 32 bits
- MSB or LSB first data transfer
- Rx and Tx on both rising or falling edge of serial clock independently
- Supports Byte Suspend mode in 32-bit transmission
- I²C
 - Master/Slave up to 1 Mbit/s
 - Bi-directional data transfer between masters and slaves
 - Multi-master bus (no central master)
 - Arbitration between simultaneously transmitting masters
 - Programmable clocks allow versatile rate control
 - Multiple address recognition (four slave address with mask option)
- CAN
 - CAN 2.0B protocol compatible device
 - Support 11-bit identifier as well as 29-bit identifier
 - Bit rates up to 1Mbits/s
 - NRZ bit Coding/ Encoding
 - Error Detection & Status Report
 - Bit error, Form error, Stuffing error, 15-bit CRC detection, and Acknowledge error Interrupt
 - Bit Timing Synchronization
 - Acceptance filter extension
- ADC
 - Two A/D converters
 - Each ADC with up to 8 channel, 12-bit resolution with 10-bit accuracy
 - 16 result registers
 - Sampling rate up to 800ksps
 - Two operating modes:
 - Single Sampling mode: Only one specified channel can be sampled at one time.
 - Simultaneous Sampling mode: Allowing two ADC channels to be sampled simultaneously.
 - Two converting result digital comparators
 - Conversion start by software, external pins, or linked with Timer 0~3 or PWM module
- Up to three Analog Comparators
- Up to two OPA (operational amplifier)
- Brown-out detector
 - 4 levels: 4.4V/3.7V/2.7V/2.2V
 - Optional brown-out interrupt or reset

- Built-in LDO for Wide Operating Voltage Range: 2.5V to 5.5V
- Low Voltage Reset
- 96-bit unique ID
- Operating Temperature: -40°C ~105°C
- Develop tools: parallel writer or In-Circuit Programming (ICP) writer
- Packages:
 - All Green package (RoHS)
 - LQFP 100/64/48-pin

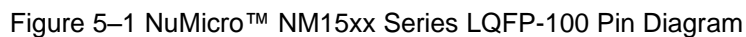
3 BLOCK DIAGRAM



4 PARTS LIST

	NM1530VE3AE NM1530VD3AE	NM1520RD2AE NM1520RC2AE	NM1520LD2AE NM1520LC2AE	NM1521RD2AE	NM1510LC1AE
AP Flash	128KB/64KB	64KB/32KB	64KB/32K	64KB	32KB
RAM	16KB	8KB	8KB	8KB	4KB
Data Flash	4KB	4KB	4KB	4KB	4KB
Timer	4 x 24-bit	4 x 24-bit	4 x 24-bit	4 x 24-bit	4 x 24-bit
PWM	6ch PWM0, 6ch PWM1 2ch PWM2	6ch PWM0, 6ch PWM1 1ch PWM2	6ch PWM0, 3ch PWM1	6ch PWM0, 6ch PWM1 1ch PWM2	6ch PWM0, 3ch PWM1
QEI IC	3ch x 2 sets(QEI0,QEI1) 3ch x 2 sets(IC0,IC1)	3ch x 1 set(QEI0,QEI1) Pin shared with QEIO	3ch x 1 set(QEI0) Pin shared with QEIO	3ch x 1 set(QEI0) 3ch x 1 set (IC1)	3ch x 1 set(QEI0) Pin shared with QEIO
UART	2	2	2	2	2
SPI	3	1	1	1	1
I2C	1	1	1	1	1
CAN 2.0B	1	1	1	1	-
ADC	8ch ADCA 8ch ADCB	7ch ADCA 7ch ADCB	5ch ADCA 4ch ADCB	4ch ADCA 7ch ADCB	5ch ADCA 4ch ADCB
Comparator	CMP0, CMP1, CMP2	CMP1, CMP2	CMP1	CMP2	CMP1
OP	OP0, OP1	OP0, OP1	OP0, OP1	OP0, OP1	OP0, OP1
Package	LQFP100(14x14x1.4mm)	LQFP64(10x10x1.4mm)	LQFP48(7x7x1.4mm)	LQFP64(10x10x1.4mm)	LQFP48(7x7x1.4mm)

5.1 LQFP 100-pin



5.2 LQFP 64-pin

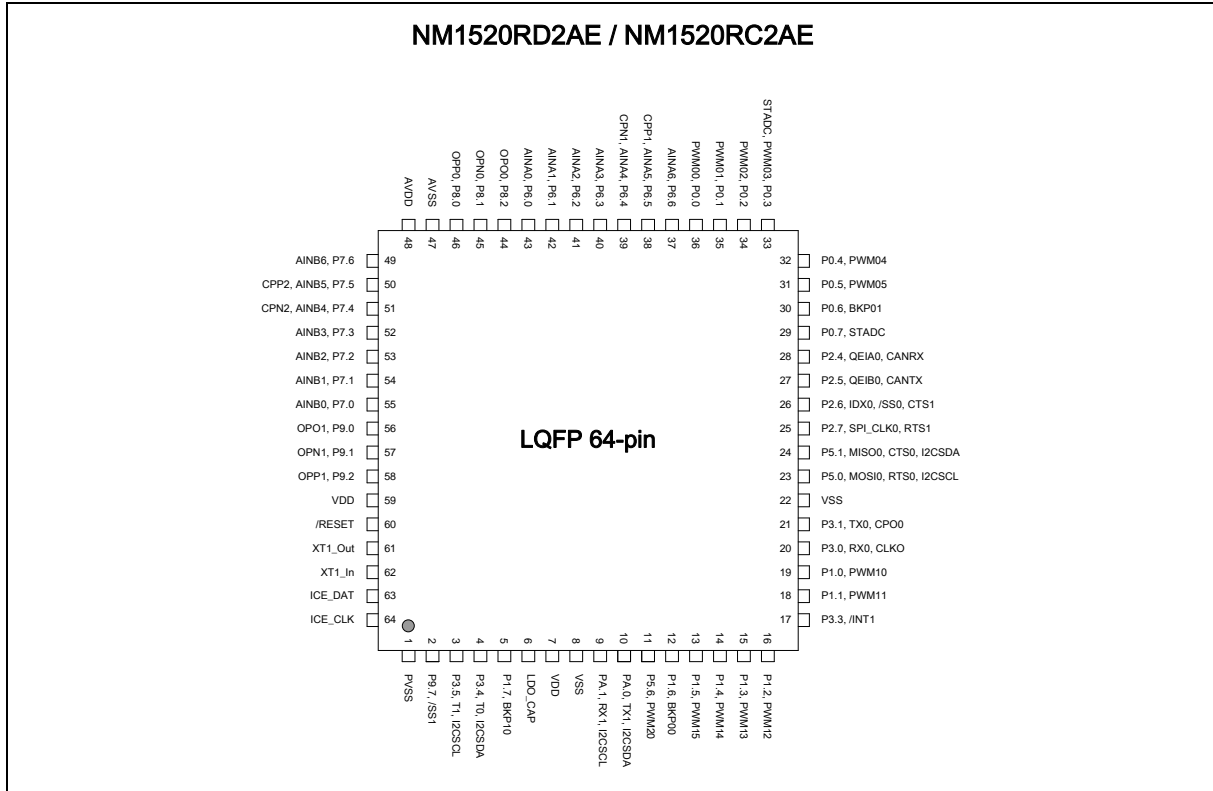


Figure 5–2 NuMicro™ NM15xx Series LQFP-64 Pin Diagram

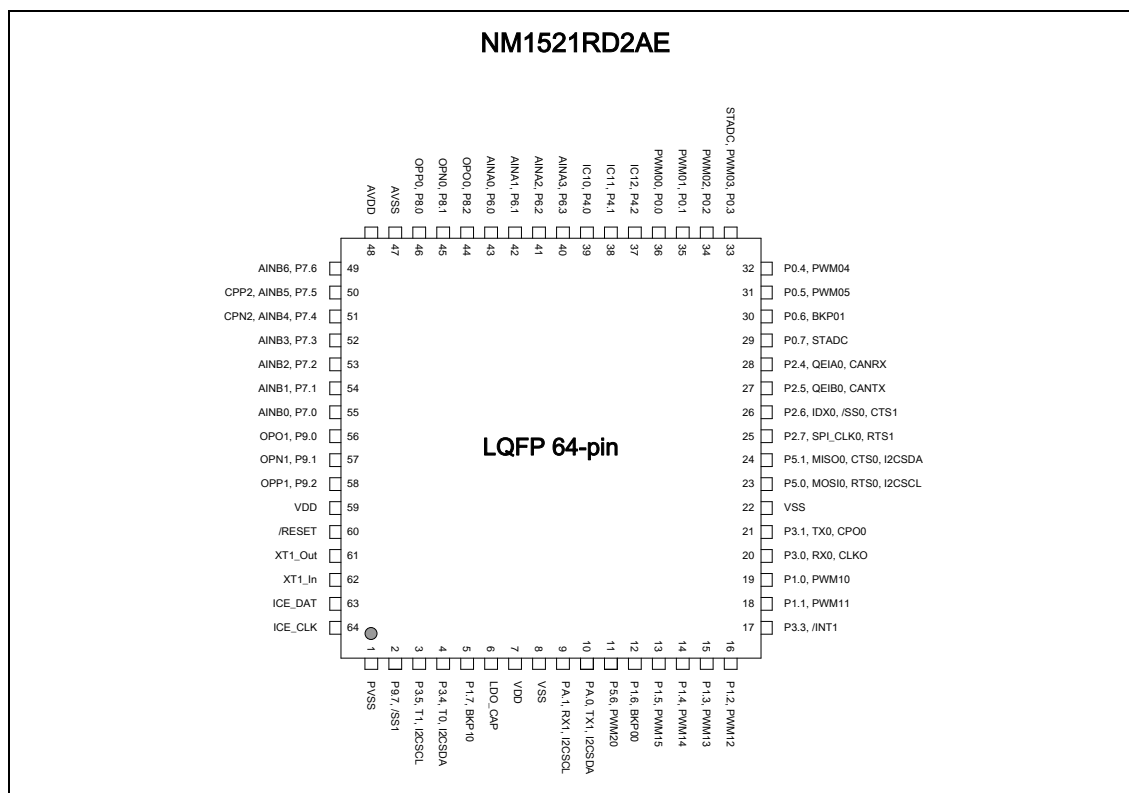


Figure 5–3 NuMicro™ NM1521 Series LQFP-64 Pin Diagram

5.3 LQFP 48-pin

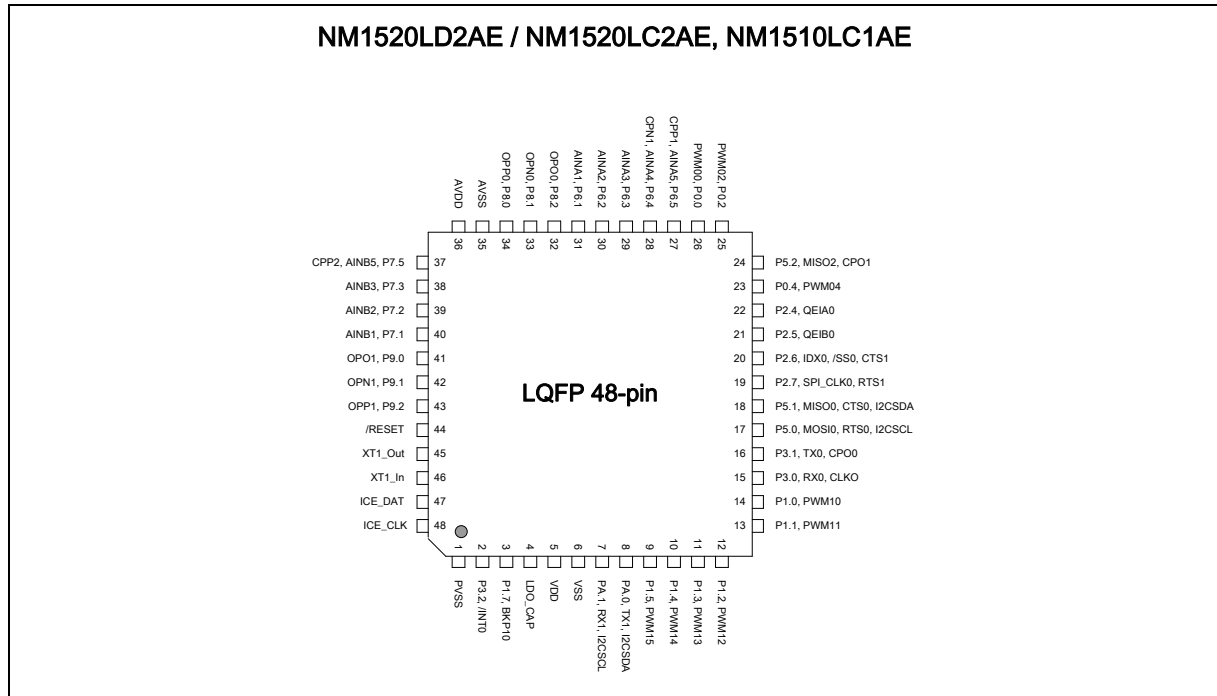


Figure 5–4 NuMicro™ NM15xx Series LQFP-48 Pin Diagram

5.4 Pin Description

Pin Number			Pin Name	Pin Type ^[1]	Description
100- pin	64-pin	48-pin			
10	7	5	V _{DD}	P	POWER SUPPLY: Supply voltage Digital V _{DD} for operation.
34					
61	59				
89					
11	8	6	V _{SS}	P	GROUND: Digital Ground potential.
35					
60	22				
90					
9	6	4	LDO_CAP	P	LDO: LDO output pin Note: It needs to be connected with a 10uF capacitor.
1	1	1	PVSS	P	PLL GROUND: PLL Ground potential.
74	48	36	AV _{DD}	AP	Power supply for internal analog circuit
73	47	35	AV _{SS}	AP	Ground Pin for analog circuit
75	-	-	Vref	AP	Voltage reference input for ADC
93	60	44	/RESET	I (ST)	RESET: /RST pin is a Schmitt trigger input pin for hardware device reset. A “ Low ” on this pin for 768 clock counter of Internal RC 22.1184 MHz while the system clock is running will reset the device. /RST pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
94	61	45	XT_OUT	O	CRYSTAL OUT: This is the output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1.
95	62	46	XT_IN	I (ST)	CRYSTAL IN: This is the input pin to the internal inverting amplifier. The system clock is from external crystal or resonator when FOSC[1:0] (CONFIG3[1:0]) are both logic 1 by default.
96	63	47	ICE_DAT	I/O	Serial Wired Debugger Data pin
97	64	48	ICE_CLK	I	Serial Wired Debugger Clock pin
57	36	26	P0.0	I/O	General purpose digital I/O pin
			PWM00	O	PWM0 output of PWM Unit 0
56	35	-	P0.1	I/O	General purpose digital I/O pin
			PWM01	O	PWM1 output of PWM Unit 0
55	34	25	P0.2	I/O	General purpose digital I/O pin
			PWM02	O	PWM2 output of PWM Unit 0
54	33	-	P0.3	I/O	General purpose digital I/O pin
			PWM03	O	PWM3 output of PWM Unit 0



Pin Number			Pin Name	Pin Type ⁽¹⁾	Description
100-pin	64-pin	48-pin			
			STADC	I	ADC external trigger input
45	32	23	P0.4	I/O	General purpose digital I/O pin
			PWM04	O	PWM4 output of PWM Unit 0
44	31	-	P0.5	I/O	General purpose digital I/O pin
			PWM05	O	PWM5 output of PWM Unit 0
43	30	-	P0.6	I/O	General purpose digital I/O pin
			BKP01	I	Brake input pin 1 of PWM Unit 0
42	29	-	P0.7	I/O	General purpose digital I/O pin
			STADC	I	ADC external trigger input
30	19	14	P1.0	I/O	General purpose digital I/O pin
			PWM10	O	PWM0 output of PWM Unit 1
29	18	13	P1.1	I/O	General purpose digital I/O pin
			PWM11	O	PWM1 output of PWM Unit 1
20	16	12	P1.2	I/O	General purpose digital I/O pin
			PWM12	O	PWM2 output of PWM Unit 1
19	15	11	P1.3	I/O	General purpose digital I/O pin
			PWM13	O	PWM3 output of PWM Unit 1
18	14	10	P1.4	I/O	General purpose digital I/O pin
			PWM14	O	PWM4 output of PWM Unit 1
17	13	9	P1.5	I/O	General purpose digital I/O pin
			PWM15	O	PWM5 output of PWM Unit 1
16	12	-	P1.6	I/O	General purpose digital I/O pin
			BKP00	I	Brake input pin 0 of PWM Unit 0
8	5	3	P1.7	I/O	General purpose digital I/O pin
			BKP10	I	Brake input pin0 of PWM Unit 1
49	-	-	P2.0	I/O	General purpose digital I/O pin
			MOSI2	I/O	SPI2 MOSI (Master Out, Slave In) pin
			CPO2	AO	Analog comparator 2 output pin
48	-	-	P2.1	I/O	General purpose digital I/O pin
			IC02	I	Input 2 of Input Capture Unit 0
47	-	-	P2.2	I/O	General purpose digital I/O pin
			IC01	I	Input 1 of Input Capture Unit 0
46	-	-	P2.3	I/O	General purpose digital I/O pin

Pin Number			Pin Name	Pin Type ^[1]	Description
100-pin	64-pin	48-pin			
			IC00	I	Input 0 of Input Capture Unit 0
41	28	22	P2.4	I/O	General purpose digital I/O pin
			QEIA0	I	Quadrature encoder phase A input of QEI Unit 10
			CANRX	I	CAN Bus RX Input (not supported in 48-pin)
40	27	21	P2.5	I/O	General purpose digital I/O pin
			QEIB0	I	Quadrature encoder phase B input of QEI Unit 0
			CANTX	O	CAN Bus TX Output (not supported in 48-pin)
39	26	20	P2.6	I/O	General purpose digital I/O pin
			IDX0	I	Quadrature Encoder Index input of QEI Unit 0
			/SS0	I/O	SPI0 slave select pin
			CTS1	I	UART1 CTS pin
38	25	19	P2.7	I/O	General purpose digital I/O pin
			SPI_CLK0	I/O	SPI0 serial clock pin
			RTS1	O	UART1 RTS pin
31	20	15	P3.0	I/O	General purpose digital I/O pin
			RX0	I	Data Receiver input pin for UART0
32	21	16	P3.1	I/O	General purpose digital I/O pin
			TX0	O	Data transmitter output pin for UART0
			CPO0	AO	Analog comparator 0 output
7	-	2	P3.2	I/O	General purpose digital I/O pin
			/INT0	I	External Interrupt 0 input pin
27	17	-	P3.3	I/O	General purpose digital I/O pin
			/INT1	I	External Interrupt 1 input pin
6	4	-	P3.4	I/O	General purpose digital I/O pin
			T0	I/O	Timer0 external clock
			I2CSDA	I/O	I2C data input/output pin
5	3	-	P3.5	I/O	General purpose digital I/O pin
			T1	I/O	Timer1 external clock
			I2CSCL	I/O	I2C clock output pin
4	-	-	P3.6	I/O	General purpose digital I/O pin
			CANRX	I	CAN Bus RX Input
3	-	-	P3.7	I/O	General purpose digital I/O pin



Pin Number			Pin Name	Pin Type ⁽¹⁾	Description
100-pin	64-pin	48-pin			
			CANTX	O	CAN Bus TX Output
23	-	-	P4.0	I/O	General purpose digital I/O pin
			IC10	I	Input 0 of Input Capture Unit 1
24	-	-	P4.1	I/O	General purpose digital I/O pin
			IC11	I	Input 1 of Input Capture Unit 1
25	-	-	P4.2	I/O	General purpose digital I/O pin
			IC12	I	Input 2 of Input Capture Unit 1
26	-	-	P4.3	I/O	General purpose digital I/O pin
21	-	-	P4.4	I/O	General purpose digital I/O pin
			QEIA1	I	Quadarature encoder phase A input of QEI Unit 1
22	-	-	P4.5	I/O	General purpose digital I/O pin
			QEIB1	I	Quadarature encoder phase B input of QEI Unit 1
28	--	-	P4.6	I/O	General purpose digital I/O pin
			T2	I/O	Timer2 external clock
			IDX1	I	Quadrature Encoder Index input of QEI Unit 1
33	-	-	P4.7	I/O	General purpose digital I/O pin
			T3	I/O	Timer3 external clock
36	23	17	P5.0	I/O	General purpose digital I/O pin
			MOSI0	I/O	SPI0 MOSI (Master Out, Slave In) pin
			RTS0	O	UART0 RTS pin
37	24	18	P5.1	I/O	General purpose digital I/O pin
			MISO0	I/O	SPI0 MISO (Master In, Slave Out) pin
			CTS0	I	UART0 CTS pin
50	-	24	P5.2	I/O	General purpose digital I/O pin
			MISO2	I/O	SPI2 MISO (Master In, Slave Out) pin
			CPO1	AO	Analog comparator 1 output pin
51	-	-	P5.3	I/O	General purpose digital I/O pin
			SPI_CLK2	I/O	SPI2 serial clock pin
52	-	-	P5.4	I/O	General purpose digital I/O pin
			/SS2	I/O	SPI2 slave select pin
53	-	-	P5.5	I/O	General purpose digital I/O pin
			CLKO	O	Frequency Divider output pin
15	11	-	P5.6	I/O	General purpose digital I/O pin

Pin Number			Pin Name	Pin Type ^[1]	Description
100-pin	64-pin	48-pin			
			PWM20	I/O	PWM0 output of PWM unit 2
14	-	-	P5.7	I/O	General purpose digital I/O pin
			PWM21	I/O	PWM1 output of PWM unit 2
69	42	-	P6.0	I/O	General purpose digital I/O pin
			AINA0	AI	ADC analog input 0 for sample-and-hold A
68	42	31	P6.1	I/O	General purpose digital I/O pin
			AINA1	AI	ADC analog input 1 for sample-and-hold A
67	41	30	P6.2	I/O	General purpose digital I/O pin
			AINA2	AI	ADC analog input 2 for sample-and-hold A
66	40	29	P6.3	I/O	General purpose digital I/O pin
			AINA3	AI	ADC analog input 3 for sample-and-hold A
65	39	28	P6.4	I/O	General purpose digital I/O pin
			AINA4	AI	ADC analog input 4 for sample-and-hold A
			CPN1	AI	Analog comparator 1 negative input
64	38	27	P6.5	I/O	General purpose digital I/O pin
			AINA5	AI	ADC analog input 5 for sample-and-hold A
			CPP1	AI	Analog comparator 1 positive input
63	37	-	P6.6	I/O	General purpose digital I/O pin
			AINA6	AI	ADC analog input 6 for sample-and-hold A
62	-	-	P6.7	I/O	General purpose digital I/O pin
			AINA7	AI	ADC analog input 7 for sample-and-hold A
83	55	-	P7.0	I/O	General purpose digital I/O pin
			AINB0	AI	ADC analog input 0 for sample-and-hold B
82	54	40	P7.1	I/O	General purpose digital I/O pin
			AINB1	AI	ADC analog input 1 for sample-and-hold B
81	53	39	P7.2	I/O	General purpose digital I/O pin
			AINB2	AI	ADC analog input 2 for sample-and-hold B
80	52	38	P7.3	I/O	General purpose digital I/O pin
			AINB3	AI	ADC analog input 3 for sample-and-hold B
79	51	-	P7.4	I/O	General purpose digital I/O pin
			AINB4	AI	ADC analog input 4 for sample-and-hold B
			CPN2	AI	Analog comparator 2 negative input



Pin Number			Pin Name	Pin Type ⁽¹⁾	Description
100-pin	64-pin	48-pin			
78	50	37	P7.5	I/O	General purpose digital I/O pin
			AINB5	AI	ADC analog input 5 for sample-and-hold B
			CPP2	AI	Analog comparator 2 positive input
77	49	-	P7.6	I/O	General purpose digital I/O pin
			AINB6	AI	ADC analog input 6 for sample-and-hold B
76	-	-	P7.7	I/O	General purpose digital I/O pin
			AINB7	AI	ADC analog input 7 for sample-and-hold B
72	46	34	P8.0	I/O	General purpose digital I/O pin
			OPP0	AI	OP Amplifier 0 positive input
71	45	33	P8.1	I/O	General purpose digital I/O pin
			OPN0	AI	OP Amplifier 0 negative input
70	44	32	P8.2	I/O	General purpose digital I/O pin
			OPO0	AO	OP Amplifier 0 output
85	-	-	P8.3	I/O	General purpose digital I/O pin
			CPN0	AI	Analog comparator negative input pin
84	-	-	P8.4	I/O	General purpose digital I/O pin
			CPP0	AI	Analog comparator positive input pin
91	-	-	P8.5	I/O	General purpose digital I/O pin
59	-	-	P8.6	I/O	General purpose digital I/O pin
58	-	-	P8.7	I/O	General purpose digital I/O pin
			CPO0	O	Analog comparator output pin
86	56	41	P9.0	I/O	General purpose digital I/O pin
			OPO1	AO	OP Amplifier 1 output
87	57	42	P9.1	I/O	General purpose digital I/O pin
			OPN1	AI	OP Amplifier 1 negative input
88	58	43	P9.2	I/O	General purpose digital I/O pin
			OPP1	AI	OP Amplifier 1 positive input
92	-	-	P9.3	I/O	General purpose digital I/O pin
			BKP11	I	Brake input pin 1 of PWM Unit 1
98	-	-	P9.4	I/O	General purpose digital I/O pin
			SPI_CLK1	I/O	SPI1 serial clock pin
99	-	-	P9.5	I/O	General purpose digital I/O pin
			MISO1	I/O	SPI1 MISO (Master In, Slave Out) pin

Pin Number			Pin Name	Pin Type ^[1]	Description
100-pin	64-pin	48-pin			
100	-	-	P9.6	I/O	General purpose digital I/O pin
			MOSI1	I/O	SPI1 MOSI (Master Out, Slave In) pin
2	2	-	P9.7	I/O	General purpose digital I/O pin
			/SS1	I/O	SPI1 slave select pin
13	10	8	PA.0	I/O	General purpose digital I/O pin
			TX1	O	Data transmitter output pin for UART1
			I2CSDA	I/O	I2C data input/output pin
12	9	7	PA.1	I/O	General purpose digital I/O pin
			RX1	I	Data Receiver input pin for UART1
			I2CSCL	I/O	I2C clock output pin

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power

6 ARM® CORTEX™-M0 CORE

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex-M profile processor. The profile supports two modes –Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 6–1 shows the functional controller of processor.

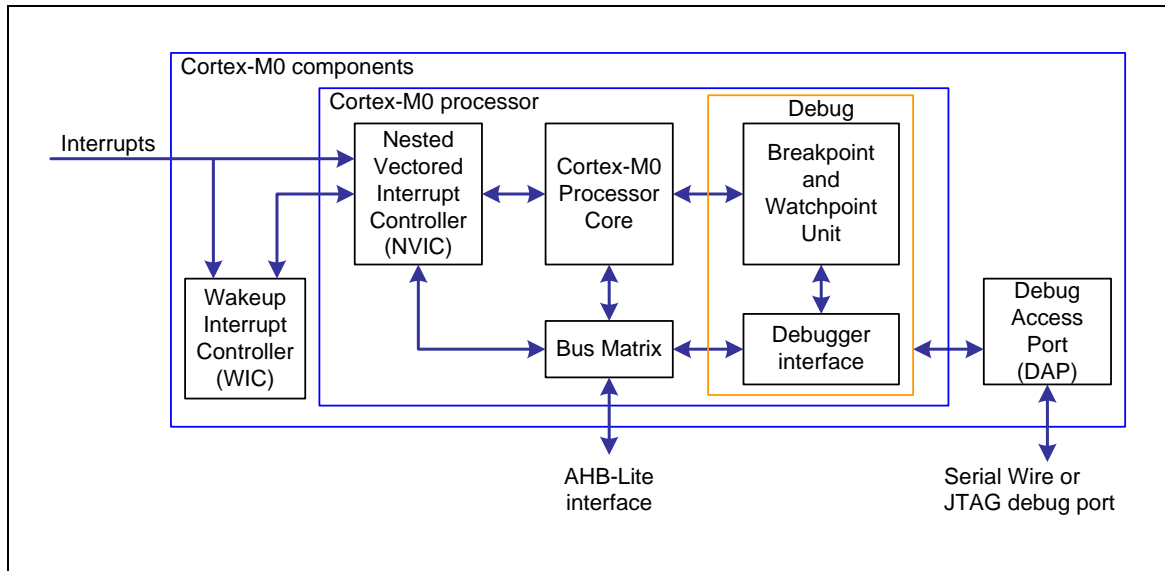


Figure 6–1 Functional Controller Diagram

The implemented device provides:

- A low gate count processor:
 - ◆ ARMv6-M Thumb® instruction set
 - ◆ Thumb-2 technology
 - ◆ ARMv6-M compliant 24-bit SysTick timer
 - ◆ A 32-bit hardware multiplier
 - ◆ The system interface supports little-endian data accesses
 - ◆ The ability to have deterministic, fixed-latency, interrupt handling
 - ◆ Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
 - ◆ C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
 - ◆ Low power sleep-mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature

- NVIC:
 - ◆ 32 external interrupt inputs, each with four levels of priority
 - ◆ Dedicated Non-Maskable Interrupt (NMI) input
 - ◆ Supports for both level-sensitive and pulse-sensitive interrupt lines
 - ◆ Supports Wake-up Interrupt Controller (WIC) and providing ultra-low power sleep mode
- Debug support:
 - ◆ Four hardware breakpoints
 - ◆ Two watchpoints
 - ◆ Program Counter Sampling Register (PCSR) for non-intrusive code profiling
 - ◆ Single step and vector catch capabilities
- Bus interfaces:
 - ◆ Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
 - ◆ Single 32-bit slave port that supports the DAP (Debug Access Port)

7 SYSTEM MANAGEMENT

7.1 Overview

System management includes the following sections:

- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset , multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

7.2 System Reset

The system reset can be issued by one of the following listed events. For these reset event flags can be read by RSTRC register.

- Hardware Reset
 - Power-On Reset (POR)
 - Low level on the Reset pin (nRST)
 - Watchdog Time-out Reset (WDT)
 - Low Voltage Reset (LVR)
 - Brown-out Detector Reset (BOD)
- Software Reset
 - MCU Reset - SYSRESETREQ (AIRC[2])
 - Cortex-M0 Core One-shot Reset - CPU_RST (IPRSTC1[1])
 - Chip One-shot Reset - CHIP_RST (IPRSTC1[0])

Note: ISPCON.BS keeps the original value after MCU Reset and Cortex-M0 Core One-shot Reset.

7.3 System Power Distribution

In this chip, the power distribution is divided into two segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the I/O pins and internal regulator which provides a fixed 1.8V power for digital operation.

The output of internal voltage regulators, LDO_CAP, requires an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}).

7.4 System Memory Map

The NuMicro™ NM15xx Series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in the following table. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip peripheral. The NuMicro™ NM15xx Series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0001_FFFF	FLASH_BA	FLASH Memory Space (128 KB)
0x2000_0000 – 0x2000_3FFF	SRAM_BA	SRAM Memory Space (16 KB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_4000 – 0x5001_7FFF	DIV_BA	Hardware Divider Register
APB1 Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4000_4100 – 0x4000_7FFF	WWDT_BA	Window Watchdog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C_BA	I ² C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	BPWM_BA	Basic PWM Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x400D_0000 – 0x400D_3FFF	ACMP_BA	Analog Comparator Control Registers
0x400E_0000 – 0x400E_3FFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
0x400F_0000 – 0x400F_3FFF	OPA_BA	Operation Amplifier Control Registers
APB2 Controllers Space (0x4010_0000 ~ 0x401F_FFFF)		



Address Space	Token	Controllers
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4013_0000 – 0x4013_3FFF	SPI2_BA	SPI2 with master/slave function Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x4018_0000 – 0x4018_3FFF	CAN_BA	CAN Bus Control Registers
0x4019_0000 – 0x4019_3FFF	EPWM0_BA	Enhanced PWM0 Control Registers
0x4019_4000 – 0x4019_7FFF	EPWM1_BA	Enhanced PWM1 Control Registers
0x401B_0000 – 0x401B_3FFF	CAP0_BA	Input Capture 0 Control Registers
0x401B_4000 – 0x401B_7FFF	CAP1_BA	Input Capture 1 Control Registers
0x401C_0000 – 0x401C_3FFF	QEI0_BA	Quadrature Encoder Interface 0 Control Registers
0x401C_4000 – 0x401C_7FFF	QEI1_BA	Quadrature Encoder Interface 1 Control Registers
0x401D_0000 – 0x401D_3FFF	MDU_BA	Motor Drive Unit Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E01F	SYST_BA	System Timer Control Registers
0xE000_E100 – 0xE000_E4EF	NVIC_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED3F	SCS_BA	System Control Registers

Table 7-1 Address Space Assignments for On-Chip Controllers

7.5 System Timer (SysTick)

The Cortex™-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “ARM® Cortex™-M0 Data Sheet” and “ARM® v6-M Architecture Reference Manual”.

7.5.1 System Timer Control Register Map

R: read only, W: write only, R/W: both read and write

Register	Offset	R/W	Description	Reset Value
SYST Base Address:				
SYST_BA = 0xE000_E010				
SYST_CSR	SYST_BA+0x00	R/W	SysTick Control and Status Register	0x0000_0000
SYST_RVR	SYST_BA+0x04	R/W	SysTick Reload Value Register	0xFFFF_FFFF
SYST_CVR	SYST_BA+0x08	R/W	SysTick Current Value Register	0xFFFF_FFFF

SysTick Control and Status (SYST_CSR)

Register	Offset	R/W	Description	Reset Value
SYST_CSR	SYST_BA+0x00	R/W	SysTick Control and Status Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							COUNTFLAG
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					CLKSRC	TICKINT	ENABLE

Bits	Description	
[31:17]	Reserved	Reserved.
[16]	COUNTFLAG	SysTick flag. COUNTFLAG is set when the counter transitions to zero. COUNTFLAG is cleared by a read from this register or a write to the SYST_CVR.
[15:3]	Reserved	Reserved.
[2]	CLKSRC	System Tick Clock Source Selection 0 = Clock source is optional, refer to STCLK_S (CLKSEL0[5:3]). 1 = Core clock used for SysTick timer.
[1]	TICKINT	Enables SysTick exception request. 0 = Counting down to zero does not assert the SysTick exception request 1 = Counting down to zero to asserts the SysTick exception request.
[0]	ENABLE	Enables SysTick counter. 0 = SysTick counter Disabled 1 = SysTick counter Enabled.

SysTick Reload Value Register (SYST_RVR)

Register	Offset	R/W	Description	Reset Value
SYST_RVR	SYST_BA+0x04	R/W	SysTick Reload Value Register	0xFFFF_FFFF

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
RELOAD[23:16]							
15	14	13	12	11	10	9	8
RELOAD[15:8]							
7	6	5	4	3	2	1	0
RELOAD[7:0]							

Bits	Description	
[31:24]	Reserved	Reserved.
[23:0]	RELOAD	System Tick Reload Value Value to load into the Current Value register when the counter reaches 0.

SysTick Current Value Register (SYST_CVR)

Register	Offset	R/W	Description	Reset Value
SYST_CVR	SYST_BA+0x08	R/W	SysTick Current Value Register	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
CURRENT[23:16]							
15	14	13	12	11	10	9	8
CURRENT[15:8]							
7	6	5	4	3	2	1	0
CURRENT[7:0]							

Bits	Description	
[31:24]	Reserved	Reserved.
[23:0]	CURRENT	System Tick Current Value Current counter value. This is the value of the counter at the time it is sampled. The counter does not provide read-modify-write protection. The register is write-clear. A software write of any value will clear the register to 0. Unsupported bits RAZ (see SysTick Reload Value register).

7.6 Nested Vectored Interrupt Controller (NVIC)

The Cortex™-M0 provides an interrupt controller as an integral part of the exception mode, named as “Nested Vectored Interrupt Controller (NVIC)”, which is closely coupled to the processor core and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in “Handler Mode”. This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers “PC, PSR, LR, R0~R3, R12” to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports “Tail Chaining” which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports “Late Arrival” which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the “ARM® Cortex™-M0 Data Sheet” and “ARM® v6-M Architecture Reference Manual”.

7.6.1 Exception Model and System Interrupt Map

Table 7-2 lists the exception model supported by the NuMicro™ NM15xx Series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0” and the lowest priority is denoted as “3”. The default priority of all the user-configurable interrupts is “0”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCALL	11	Configurable
Reserved	12 ~ 13	Reserved

Exception Name	Vector Number	Priority
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 7-2 Exception Model

Exception Number	Vector Address	Interrupt Number (Bit in Interrupt Registers)	Interrupt Name	Source Module	Exception description	Power Down wake-up
1 ~ 15		-	-	-	System exceptions	-
16	0x40	0	BOD_INT	Brown-Out	Brown-Out low voltage detected interrupt	Yes
17	0x44	1	WDT_INT	WDT	Watchdog Timer interrupt	Yes
18	0x48	2	EINT0_INT	P3.2	External signal interrupt from P3.2 pin	Yes
19	0x4C	3	EINT1_INT	P3.3	External signal interrupt from P3.3 pin	Yes
20	0x50	4	GPG0_INT	P0~P4 except P3.2 and P3.3	External interrupt from GPIO group 0 (P0~P4) except P3.2 and P3.3	Yes
21	0x54	5	GPG1_INT	P5~PA	External interrupt from GPIO group 1 (P5~PA)	Yes
22	0x58	6	BPWM_INT	BPWM0/1	Basic PWM0 and PWM1 interrupt	No
23	0x5C	7	ADC0_INT	ADC0	ADC0 interrupt	No
24	0x60	8	TMR0_INT	TMR0	Timer 0 interrupt	No
25	0x64	9	TMR1_INT	TMR1	Timer 1 interrupt	No
26	0x68	10	TMR2_INT	TMR2	Timer 2 interrupt	No
27	0x6C	11	TMR3_INT	TMR3	Timer 3 interrupt	No
28	0x70	12	UART0_INT	UART0	UART0 interrupt	Yes
29	0x74	13	UART1_INT	UART1	UART1 interrupt	Yes
30	0x78	14	SPI0_INT	SPI0	SPI0 interrupt	No
31	0x7C	15	SPI1_INT	SPI1	SPI1 interrupt	No
32	0x80	16	SPI2_INT	SPI2	SPI2 interrupt	No
33	0x84	17	MDU_INT	MDU	Motor drive unit interrupt	No
34	0x88	18	I2C_INT	I ² C	I ² C interrupt	Yes
35	0x8C	19	CKD_INT	CKD	CKD interrupt	No

Exception Number	Vector Address	Interrupt Number (Bit in Interrupt Registers)	Interrupt Name	Source Module	Exception description	Power Down wake-up
36	0x90	20	CAN_INT	CAN	CAN interrupt	No
37	0x94	21	EPWM0_INT	EPWM0	Enhanced PWM0 interrupt	No
38	0x98	22	EPWM1_INT	EPWM1	Enhanced PWM1 interrupt	No
39	0x9C	23	CAP0_INT	CAP0	Input capture 0 interrupt	No
40	0xA0	24	CAP1_INT	CAP1	Input capture 1 interrupt	No
41	0xA4	25	ACMP_INT	ACMP	Analog Comparator 0 or 1, or OP Amplifier digital output interrupt	Yes (only by analog comparator)
42	0xA8	26	QEI0_INT	QEI0	QEI0 interrupt	No
43	0xAC	27	QEI1_INT	QEI1	QEI1 interrupt	No
44	0xB0	28	PWRWU_INT	CLKC	Clock controller interrupt for chip wake up from power-down state	-
45	0xB4	29	ADC1_INT	ADC1	ADC1 interrupt	No
46	0xB8	30	ADC2_INT	ADC2	ADC2 interrupt	No
47	0xBC	31	ADC3_INT	ADC3	ADC3 interrupt	No

Table 7-3 System Interrupt Map Vector Table

7.6.2 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset (Bytes)	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 7-4 Vector Table

7.6.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not be activated. If an interrupt is Active when it is disabled, it

remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

7.6.4 NVIC Control Registers

R: read only, W: write only, R/W: both read and write

Register	Offset	R/W	Description	Reset Value
NVIC Base Address:				
NVIC_BA = 0xE000_E100				
NVIC_ISER	NVIC_BA+0x000	R/W	IRQ0 ~ IRQ31 Set-Enable Control Register	0x0000_0000
NVIC_ICER	NVIC_BA+0x080	R/W	IRQ0 ~ IRQ31 Clear-Enable Control Register	0x0000_0000
NVIC_ISPR	NVIC_BA+0x100	R/W	IRQ0 ~ IRQ31 Set-Pending Control Register	0x0000_0000
NVIC_ICPR	NVIC_BA+0x180	R/W	IRQ0 ~ IRQ31 Clear-Pending Control Register	0x0000_0000
NVIC_IPR0	NVIC_BA+0x300	R/W	IRQ0 ~ IRQ3 Interrupt Priority Control Register	0x0000_0000
NVIC_IPR1	NVIC_BA+0x304	R/W	IRQ4 ~ IRQ7 Interrupt Priority Control Register	0x0000_0000
NVIC_IPR2	NVIC_BA+0x308	R/W	IRQ8 ~ IRQ11 Interrupt Priority Control Register	0x0000_0000
NVIC_IPR3	NVIC_BA+0x30C	R/W	IRQ12 ~ IRQ15 Interrupt Priority Control Register	0x0000_0000
NVIC_IPR4	NVIC_BA+0x310	R/W	IRQ16 ~ IRQ19 Interrupt Priority Control Register	0x0000_0000
NVIC_IPR5	NVIC_BA+0x314	R/W	IRQ20 ~ IRQ23 Interrupt Priority Control Register	0x0000_0000
NVIC_IPR6	NVIC_BA+0x318	R/W	IRQ24 ~ IRQ27 Interrupt Priority Control Register	0x0000_0000
NVIC_IPR7	NVIC_BA+0x31C	R/W	IRQ28 ~ IRQ31 Interrupt Priority Control Register	0x0000_0000

IRQ0 ~ IRQ31 Set-Enable Control Register (NVIC_ISER)

Register	Offset	R/W	Description	Reset Value
NVIC_ISER	NVIC_BA+0x000	R/W	IRQ0 ~ IRQ31 Set-Enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETENA[31:24]							
23	22	21	20	19	18	17	16
SETENA[23:16]							
15	14	13	12	11	10	9	8
SETENA[15:8]							
7	6	5	4	3	2	1	0
SETENA[7:0]							

Bits	Description	
[31:0]	SETENA	<p>Interrupt Enable</p> <p>The ISER enables interrupts, and shows the interrupts that are enabled. Each bit represents an IRQ number from IRQ0 ~ IRQ31 (Exception number from 16 ~ 47).</p> <p>Write:</p> <p>0 = No effect.</p> <p>1 = Interrupt Enabled.</p> <p>Read:</p> <p>0 = Interrupt Disabled.</p> <p>1 = Interrupt Enabled.</p>

IRQ0 ~ IRQ31 Clear-Enable Control Register (NVIC_ICER)

Register	Offset	R/W	Description	Reset Value
NVIC_ICER	NVIC_BA+0x080	R/W	IRQ0 ~ IRQ31 Clear-Enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CLRENA[31:24]							
23	22	21	20	19	18	17	16
CLRENA[23:16]							
15	14	13	12	11	10	9	8
CLRENA[15:8]							
7	6	5	4	3	2	1	0
CLRENA[7:0]							

Bits	Description
[31:0]	<p>CLRENA</p> <p>Interrupt Clear Enable</p> <p>The ICER disables interrupts, and shows the interrupts that are enabled. Each bit represents an IRQ number from IRQ0 ~ IRQ31 (Exception number from 16 ~ 47).</p> <p>Write:</p> <p>0 = No effect.</p> <p>1 = Interrupt Disabled.</p> <p>Read:</p> <p>0 = Interrupt Disabled.</p> <p>1 = Interrupt Enabled.</p>

IRQ0 ~ IRQ31 Set-Pending Control Register (NVIC_ISPR)

Register	Offset	R/W	Description	Reset Value
NVIC_ISPR	NVIC_BA+0x100	R/W	IRQ0 ~ IRQ31 Set-Pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETPEND[31:24]							
23	22	21	20	19	18	17	16
SETPEND[23:16]							
15	14	13	12	11	10	9	8
SETPEND[15:8]							
7	6	5	4	3	2	1	0
SETPEND[7:0]							

Bits	Description
[31:0]	<p>SETPEND</p> <p>Interrupt set-pending.</p> <p>The ISPR forces interrupts into the pending state, and shows the interrupts that are pending. Each bit represents an IRQ number from IRQ0 ~ IRQ31 (Exception number from 16 ~ 47).</p> <p>Write:</p> <p>0 = no effect.</p> <p>1 = changes interrupt state to pending.</p> <p>Read:</p> <p>0 = interrupt is not pending.</p> <p>1 = interrupt is pending.</p>

IRQ0 ~ IRQ31 Clear-Pending Control Register (NVIC_ICPR)

Register	Offset	R/W	Description	Reset Value
NVIC_ICPR	NVIC_BA+0x180	R/W	IRQ0 ~ IRQ31 Clear-Pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CLRPEND[31:24]							
23	22	21	20	19	18	17	16
CLRPEND[23:16]							
15	14	13	12	11	10	9	8
CLRPEND[15:8]							
7	6	5	4	3	2	1	0
CLRPEND[7:0]							

Bits	Description
[31:0]	<p>CLRPEND</p> <p>Interrupt clear-pending.</p> <p>The ICPR removes the pending state from interrupts, and shows the interrupts that are pending. Each bit represents an IRQ number from IRQ0 ~ IRQ31 (Exception number from 16 ~ 47).</p> <p>Write:</p> <p>0 = no effect.</p> <p>1 = removes pending state an interrupt.</p> <p>Read:</p> <p>0 = interrupt is not pending.</p> <p>1 = interrupt is pending.</p>

IRQ0 ~ IRQ3 Interrupt Priority Register (NVIC_IPR0)

Register	Offset	R/W	Description	Reset Value
NVIC_IPR0	NVIC_BA+0x300	R/W	IRQ0 ~ IRQ3 Interrupt Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_3		Reserved					
23	22	21	20	19	18	17	16
PRI_2		Reserved					
15	14	13	12	11	10	9	8
PRI_1		Reserved					
7	6	5	4	3	2	1	0
PRI_0		Reserved					

Bits	Description	
[31:30]	PRI_3	Priority of IRQ3 “0” denotes the highest priority and “3” denotes lowest priority
[29:24]	Reserved	Reserved
[23:22]	PRI_2	Priority of IRQ2 “0” denotes the highest priority and “3” denotes lowest priority
[21:16]	Reserved	Reserved
[15:14]	PRI_1	Priority of IRQ1 “0” denotes the highest priority and “3” denotes lowest priority
[13:8]	Reserved	Reserved
[7:6]	PRI_0	Priority of IRQ0 “0” denotes the highest priority and “3” denotes lowest priority
[5:0]	Reserved	Reserved

IRQ4 ~ IRQ7 Interrupt Priority Register (NVIC IPR1)

Register	Offset	R/W	Description	Reset Value
NVIC_IPR1	NVIC_BA+0x304	R/W	IRQ4 ~ IRQ7 Interrupt Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_7		Reserved					
23	22	21	20	19	18	17	16
PRI_6		Reserved					
15	14	13	12	11	10	9	8
PRI_5		Reserved					
7	6	5	4	3	2	1	0
PRI_4		Reserved					

Bits	Description	
[31:30]	PRI_7	Priority of IRQ7 “0” denotes the highest priority and “3” denotes lowest priority
[29:24]	Reserved	Reserved
[23:22]	PRI_6	Priority of IRQ6 “0” denotes the highest priority and “3” denotes lowest priority
[21:16]	Reserved	Reserved
[15:14]	PRI_5	Priority of IRQ5 “0” denotes the highest priority and “3” denotes lowest priority
[13:8]	Reserved	Reserved
[7:6]	PRI_4	Priority of IRQ4 “0” denotes the highest priority and “3” denotes lowest priority
[5:0]	Reserved	Reserved

IRQ8 ~ IRQ11 Interrupt Priority Register (NVIC_IPR2)

Register	Offset	R/W	Description	Reset Value
NVIC_IPR2	NVIC_BA+0x308	R/W	IRQ8 ~ IRQ11 Interrupt Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_11		Reserved					
23	22	21	20	19	18	17	16
PRI_10		Reserved					
15	14	13	12	11	10	9	8
PRI_9		Reserved					
7	6	5	4	3	2	1	0
PRI_8		Reserved					

Bits	Description	
[31:30]	PRI_11	Priority of IRQ11 “0” denotes the highest priority and “3” denotes lowest priority
[29:24]	Reserved	Reserved
[23:22]	PRI_10	Priority of IRQ10 “0” denotes the highest priority and “3” denotes lowest priority
[21:16]	Reserved	Reserved
[15:14]	PRI_9	Priority of IRQ9 “0” denotes the highest priority and “3” denotes lowest priority
[13:8]	Reserved	Reserved
[7:6]	PRI_8	Priority of IRQ8 “0” denotes the highest priority and “3” denotes lowest priority
[5:0]	Reserved	Reserved

IRQ12 ~ IRQ15 Interrupt Priority Register (NVIC_IPR3)

Register	Offset	R/W	Description	Reset Value
NVIC_IPR3	NVIC_BA+0x30C	R/W	IRQ12 ~ IRQ15 Interrupt Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_15		Reserved					
23	22	21	20	19	18	17	16
PRI_14		Reserved					
15	14	13	12	11	10	9	8
PRI_13		Reserved					
7	6	5	4	3	2	1	0
PRI_12		Reserved					

Bits	Description	
[31:30]	PRI_15	Priority of IRQ15 “0” denotes the highest priority and “3” denotes lowest priority
[29:24]	Reserved	Reserved
[23:22]	PRI_14	Priority of IRQ14 “0” denotes the highest priority and “3” denotes lowest priority
[21:16]	Reserved	Reserved
[15:14]	PRI_13	Priority of IRQ13 “0” denotes the highest priority and “3” denotes lowest priority
[13:8]	Reserved	Reserved
[7:6]	PRI_12	Priority of IRQ12 “0” denotes the highest priority and “3” denotes lowest priority
[5:0]	Reserved	Reserved

IRQ16 ~ IRQ19 Interrupt Priority Register (NVIC_IPR4)

Register	Offset	R/W	Description	Reset Value
NVIC_IPR4	NVIC_BA+0x310	R/W	IRQ16 ~ IRQ19 Interrupt Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_19		Reserved					
23	22	21	20	19	18	17	16
PRI_18		Reserved					
15	14	13	12	11	10	9	8
PRI_17		Reserved					
7	6	5	4	3	2	1	0
PRI_16		Reserved					

Bits	Description	
[31:30]	PRI_19	Priority of IRQ19 "0" denotes the highest priority and "3" denotes lowest priority
[29:24]	Reserved	Reserved
[23:22]	PRI_18	Priority of IRQ18 "0" denotes the highest priority and "3" denotes lowest priority
[21:16]	Reserved	Reserved
[15:14]	PRI_17	Priority of IRQ17 "0" denotes the highest priority and "3" denotes lowest priority
[13:8]	Reserved	Reserved
[7:6]	PRI_16	Priority of IRQ16 "0" denotes the highest priority and "3" denotes lowest priority
[5:0]	Reserved	Reserved

IRQ20 ~ IRQ23 Interrupt Priority Register (NVIC_IPR5)

Register	Offset	R/W	Description	Reset Value
NVIC_IPR5	NVIC_BA+0x314	R/W	IRQ20 ~ IRQ23 Interrupt Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_23		Reserved					
23	22	21	20	19	18	17	16
PRI_22		Reserved					
15	14	13	12	11	10	9	8
PRI_21		Reserved					
7	6	5	4	3	2	1	0
PRI_20		Reserved					

Bits	Description	
[31:30]	PRI_23	Priority of IRQ23 “0” denotes the highest priority and “3” denotes lowest priority
[29:24]	Reserved	Reserved
[23:22]	PRI_22	Priority of IRQ22 “0” denotes the highest priority and “3” denotes lowest priority
[21:16]	Reserved	Reserved
[15:14]	PRI_21	Priority of IRQ21 “0” denotes the highest priority and “3” denotes lowest priority
[13:8]	Reserved	Reserved
[7:6]	PRI_20	Priority of IRQ20 “0” denotes the highest priority and “3” denotes lowest priority
[5:0]	Reserved	Reserved

IRQ24 ~ IRQ27 Interrupt Priority Register (NVIC_IPR6)

Register	Offset	R/W	Description	Reset Value
NVIC_IPR6	NVIC_BA+0x318	R/W	IRQ24 ~ IRQ27 Interrupt Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_27		Reserved					
23	22	21	20	19	18	17	16
PRI_26		Reserved					
15	14	13	12	11	10	9	8
PRI_25		Reserved					
7	6	5	4	3	2	1	0
PRI_24		Reserved					

Bits	Description	
[31:30]	PRI_27	Priority of IRQ27 “0” denotes the highest priority and “3” denotes lowest priority
[29:24]	Reserved	Reserved
[23:22]	PRI_26	Priority of IRQ26 “0” denotes the highest priority and “3” denotes lowest priority
[21:16]	Reserved	Reserved
[15:14]	PRI_25	Priority of IRQ25 “0” denotes the highest priority and “3” denotes lowest priority
[13:8]	Reserved	Reserved
[7:6]	PRI_24	Priority of IRQ24 “0” denotes the highest priority and “3” denotes lowest priority
[5:0]	Reserved	Reserved

IRQ28 ~ IRQ31 Interrupt Priority Register (NVIC_IPR7)

Register	Offset	R/W	Description	Reset Value
NVIC_IPR7	NVIC_BA+0x31C	R/W	IRQ28 ~ IRQ31 Interrupt Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_31		Reserved					
23	22	21	20	19	18	17	16
PRI_30		Reserved					
15	14	13	12	11	10	9	8
PRI_29		Reserved					
7	6	5	4	3	2	1	0
PRI_28		Reserved					

Bits	Description	
[31:30]	PRI_31	Priority of IRQ31 “0” denotes the highest priority and “3” denotes lowest priority
[29:24]	Reserved	Reserved
[23:22]	PRI_30	Priority of IRQ30 “0” denotes the highest priority and “3” denotes lowest priority
[21:16]	Reserved	Reserved
[15:14]	PRI_29	Priority of IRQ29 “0” denotes the highest priority and “3” denotes lowest priority
[13:8]	Reserved	Reserved
[7:6]	PRI_28	Priority of IRQ28 “0” denotes the highest priority and “3” denotes lowest priority
[5:0]	Reserved	Reserved

7.6.5 Interrupt Source Control Registers

Besides the interrupt control registers associated with the NVIC, NuMicro™ NM15xx Series also implement some specific control registers to facilitate the interrupt functions, including “interrupt source identification”, “NMI source selection” and “interrupt test mode”, as described below.

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
INT Base Address:				
INT_BA = 0x5000_0300				
IRQ0_SRC	INT_BA+0x00	R	IRQ0 (BOD) interrupt source identity	0xFFFF_XXXX
IRQ1_SRC	INT_BA+0x04	R	IRQ1 (WDT) interrupt source identity	0xFFFF_XXXX
IRQ2_SRC	INT_BA+0x08	R	IRQ2 (EINT0) interrupt source identity	0xFFFF_XXXX
IRQ3_SRC	INT_BA+0x0C	R	IRQ3 (EINT1) interrupt source identity	0xFFFF_XXXX
IRQ4_SRC	INT_BA+0x10	R	IRQ4 (P0-P4) interrupt source identity	0xFFFF_XXXX
IRQ5_SRC	INT_BA+0x14	R	IRQ5 (P5-PA) interrupt source identity	0xFFFF_XXXX
IRQ6_SRC	INT_BA+0x18	R	IRQ6 (BPWM) interrupt source identity	0xFFFF_XXXX
IRQ7_SRC	INT_BA+0x1C	R	IRQ7 (ADC0) interrupt source identity	0xFFFF_XXXX
IRQ8_SRC	INT_BA+0x20	R	IRQ8 (TMR0) interrupt source identity	0xFFFF_XXXX
IRQ9_SRC	INT_BA+0x24	R	IRQ9 (TMR1) interrupt source identity	0xFFFF_XXXX
IRQ10_SRC	INT_BA+0x28	R	IRQ10 (TMR2) interrupt source identity	0xFFFF_XXXX
IRQ11_SRC	INT_BA+0x2C	R	IRQ11 (TMR3) interrupt source identity	0xFFFF_XXXX
IRQ12_SRC	INT_BA+0x30	R	IRQ12 (UART0) interrupt source identity	0xFFFF_XXXX
IRQ13_SRC	INT_BA+0x34	R	IRQ13 (UART1) interrupt source identity	0xFFFF_XXXX
IRQ14_SRC	INT_BA+0x38	R	IRQ14 (SPI0) interrupt source identity	0xFFFF_XXXX
IRQ15_SRC	INT_BA+0x3C	R	IRQ15 (SPI1) interrupt source identity	0xFFFF_XXXX
IRQ16_SRC	INT_BA+0x40	R	IRQ16 (SPI2) interrupt source identity	0xFFFF_XXXX
IRQ17_SRC	INT_BA+0x44	R	IRQ17 (MDU) interrupt source identity	0xFFFF_XXXX
IRQ18_SRC	INT_BA+0x48	R	IRQ18 (I ² C) interrupt source identity	0xFFFF_XXXX
IRQ19_SRC	INT_BA+0x4C	R	IRQ19 (CKD) interrupt source identity	0xFFFF_XXXX
IRQ20_SRC	INT_BA+0x50	R	IRQ20 (CAN) interrupt source identity	0xFFFF_XXXX
IRQ21_SRC	INT_BA+0x54	R	IRQ21 (EPWM0) interrupt source identity	0xFFFF_XXXX
IRQ22_SRC	INT_BA+0x58	R	IRQ22 (EPWM1) interrupt source identity	0xFFFF_XXXX



IRQ23_SRC	INT_BA+0x5C	R	IRQ23 (CAP0) interrupt source identity	0XXXXX_XXXX
IRQ24_SRC	INT_BA+0x60	R	IRQ24 (CAP1) interrupt source identity	0XXXXX_XXXX
IRQ25_SRC	INT_BA+0x64	R	IRQ25 (ACMP) interrupt source identity	0XXXXX_XXXX
IRQ26_SRC	INT_BA+0x68	R	IRQ26 (QE10) interrupt source identity	0XXXXX_XXXX
IRQ27_SRC	INT_BA+0x6C	R	IRQ27 (QE11) interrupt source identity	0XXXXX_XXXX
IRQ28_SRC	INT_BA+0x70	R	IRQ28 (PWRWU) interrupt source identity	0XXXXX_XXXX
IRQ29_SRC	INT_BA+0x74	R	IRQ29 (ADC1) interrupt source identity	0XXXXX_XXXX
IRQ30_SRC	INT_BA+0x78	R	IRQ30 (ADC2) interrupt source identity	0XXXXX_XXXX
IRQ31_SRC	INT_BA+0x7C	R	IRQ31 (ADC3) interrupt source identity	0XXXXX_XXXX
NMI_SEL	INT_BA+0x80	R/W	NMI Interrupt Source Select Control Register	0x0000_0000
MCU_IRQ	INT_BA+0x84	R/W	MCU interrupt request source register	0x0000_0000
MCU_IRQCR	INT_BA+0x88	R/W	MCU Interrupt Request Control Register	0x0000_0000

IRQ0 (BOD) interrupt source identity (IRQ0_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ0_SRC	INT_BA+0x00	R	IRQ0 (BOD) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							BOD_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	BOD_INT	Identify BOD interrupt source.

IRQ1 (WDT) interrupt source identity (IRQ1_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ1_SRC	INT_BA+0x04	R	IRQ1 (WDT) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						WWDT_INT	WDT_INT

Bits	Description	
[31:2]	Reserved	Reserved
[1]	WWDT_INT	Identify WWDT interrupt source.
[0]	WDT_INT	Identify WDT interrupt source.

IRQ2 (EINT0) interrupt source identity (IRQ2_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ2_SRC	INT_BA+0x08	R	IRQ2 (EINT0) interrupt source identity	0XXXXX_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							EINT0

Bits	Description	
[31:1]	Reserved	Reserved
[0]	EINT0	Identify EINT0 interrupt source. EINT0 is external interrupt 0 from P3.2.

IRQ3 (EINT1) interrupt source identity (IRQ3_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ3_SRC	INT_BA+0x0C	R	IRQ3 (EINT1) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							EINT1

Bits	Description	
[31:1]	Reserved	Reserved
[0]	EINT1	Identify EINT1 interrupt source. EINT1 is external interrupt from P3.3.

IRQ4 (P0-P4) interrupt source identity (IRQ4_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ4_SRC	INT_BA+0x10	R	IRQ4 (P0-P4) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved			P4_INT	P3_INT	P2_INT	P1_INT	P0_INT

Bits	Description	
[31:5]	Reserved	Reserved
[4]	P4_INT	Identify P4 interrupt source.
[3]	P3_INT	Identify P3 interrupt source.
[2]	P2_INT	Identify P2 interrupt source.
[1]	P1_INT	Identify P1 interrupt source.
[0]	P0_INT	Identify P0 interrupt source.

IRQ5 (P5-PA) interrupt source identity (IRQ5_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ5_SRC	INT_BA+0x14	R	IRQ5 (P5-PA) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		PA_INT	P9_INT	P8_INT	P7_INT	P6_INT	P5_INT

Bits	Description	
[31:6]	Reserved	Reserved
[5]	PA_INT	Identify PA interrupt source.
[4]	P9_INT	Identify P9 interrupt source.
[3]	P8_INT	Identify P8 interrupt source.
[2]	P7_INT	Identify P7 interrupt source.
[1]	P6_INT	Identify P6 interrupt source.
[0]	P5_INT	Identify P5 interrupt source.

IRQ6 (BPWM) interrupt source identity (IRQ6_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ6_SRC	INT_BA+0x18	R	IRQ6 (BPWM) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						BPMW1_INT	BPMW0_INT

Bits	Description	
[31:2]	Reserved	Reserved
[1]	BPWM1_INT	Identify BPWM1 interrupt source.
[0]	BPWM0_INT	Identify BPWM0 interrupt source.

IRQ7 (ADC0) interrupt source identity (IRQ7_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ7_SRC	INT_BA+0x1C	R	IRQ7 (ADC0) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							ADC0_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	ADC0_INT	Identify ADC0 interrupt source.

IRQ8 (TMR0) interrupt source identity (IRQ8_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ8_SRC	INT_BA+0x20	R	IRQ8 (TMR0) interrupt source identity	0XXXXX_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TMR0_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	TMR0_INT	Identify TMR0 interrupt source.

IRQ9 (TMR1) interrupt source identity (IRQ9_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ9_SRC	INT_BA+0x24	R	IRQ9 (TMR1) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TMR1_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	TMR1_INT	Identify TMR1 interrupt source.

IRQ10 (TMR2) interrupt source identity (IRQ10_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ10_SRC	INT_BA+0x28	R	IRQ10 (TMR2) interrupt source identity	0XXXXX_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TMR2_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	TMR2_INT	Identify TMR2 interrupt source.

IRQ11 (TMR3) interrupt source identity (IRQ11_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ11_SRC	INT_BA+0x2C	R	IRQ11 (TMR3) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							TMR3_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	TMR3_INT	Identify TMR3 interrupt source.

IRQ12 (UART0) interrupt source identity (IRQ12_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ12_SRC	INT_BA+0x30	R	IRQ12 (UART0) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							UART0_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	UART0_INT	Identify UART0 interrupt source.

IRQ13 (UART1) interrupt source identity (IRQ13_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ13_SRC	INT_BA+0x34	R	IRQ13 (UART1) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							UART1_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	UART1_INT	Identify UART1 interrupt source.

IRQ14 (SPI0) interrupt source identity (IRQ14_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ14_SRC	INT_BA+0x38	R	IRQ14 (SPI0) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							SPI0_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	SPI0_INT	Identify SPI0 interrupt source.

IRQ15 (SPI1) interrupt source identity (IRQ15_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ15_SRC	INT_BA+0x3C	R	IRQ15 (SPI1) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							SPI1_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	SPI1_INT	Identify SPI1 interrupt source.

IRQ16 (SPI2) interrupt source identity (IRQ16_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ16_SRC	INT_BA+0x40	R	IRQ16 (SPI2) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							SPI2_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	SPI2_INT	Identify SPI2 interrupt source.

IRQ17 (MDU) interrupt source identity (IRQ17_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ17_SRC	INT_BA+0x44	R	IRQ17 (MDU) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							MDU_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	MDU_INT	Identify MDU interrupt source.

IRQ18 (I2C) interrupt source identity (IRQ18_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ18_SRC	INT_BA+0x48	R	IRQ18 (I2C) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							I2C_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	I2C_INT	Identify I2C0 interrupt source.

IRQ20 (CAN) interrupt source identity (IRQ20_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ20_SRC	INT_BA+0x50	R	IRQ20 (CAN) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							CAN_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	CAN_INT	Identify CAN interrupt source.

IRQ21 (EPWM0) interrupt source identity (IRQ21_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ21_SRC	INT_BA+0x54	R	IRQ21 (EPWM0) interrupt source identity	0XXXXX_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							EPWM0_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	EPWM0_INT	Identify EPWM0 interrupt source.

IRQ22 (EPWM1) interrupt source identity (IRQ22_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ22_SRC	INT_BA+0x58	R	IRQ22 (EPWM1) interrupt source identity	0XXXXX_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							EPWM1_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	EPWM1_INT	Identify EPWM1 interrupt source.

IRQ23 (CAP0) interrupt source identity (IRQ23_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ23_SRC	INT_BA+0x5C	R	IRQ23 (CAP0) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							CAP0_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	CAP0_INT	Identify CAP0 interrupt source.

IRQ24 (CAP1) interrupt source identity (IRQ24_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ24_SRC	INT_BA+0x60	R	IRQ24 (CAP1) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							CAP1_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	CAP1_INT	Identify CAP1 interrupt source.

IRQ25 (ACMP) interrupt source identity (IRQ25_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ25_SRC	INT_BA+0x64	R	IRQ25 (ACMP) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							ACMP_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	ACMP_INT	Identify ACMP interrupt source.

IRQ26 (QEIO) interrupt source identity (IRQ26_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ26_SRC	INT_BA+0x68	R	IRQ26 (QEIO) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							QEIO_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	QEIO_INT	Identify QEIO interrupt source.

IRQ27 (QE1) interrupt source identity (IRQ27_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ27_SRC	INT_BA+0x6C	R	IRQ27 (QE1) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							QE1

Bits	Description	
[31:1]	Reserved	Reserved
[0]	QE1_INT	Identify QE1 interrupt source.

IRQ28 (PWRWU) interrupt source identity (IRQ28_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ28_SRC	INT_BA+0x70	R	IRQ28 (PWRWU) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							PWRWU_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	PWRWU_INT	Identify PWRWU interrupt source.

IRQ29 (ADC1) interrupt source identity (IRQ29_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ29_SRC	INT_BA+0x74	R	IRQ29 (ADC1) interrupt source identity	0xFFFF_FFFF

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							ADC1_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	ADC1_INT	Identify ADC1 interrupt source.

IRQ30 (ADC2) interrupt source identity (IRQ30_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ30_SRC	INT_BA+0x78	R	IRQ30 (ADC2) interrupt source identity	0xFFFF_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							ADC2_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	ADC2_INT	Identify ADC2 interrupt source.

IRQ31 (ADC3) interrupt source identity (IRQ31_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ31_SRC	INT_BA+0x7C	R	IRQ31 (ADC3) interrupt source identity	0xFFFF_FFFF

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							ADC3_INT

Bits	Description	
[31:1]	Reserved	Reserved
[0]	ADC3_INT	Identify ADC3 interrupt source.

NMI Interrupt Source Select Control Register (NMI_SEL)

Register	Offset	R/W	Description	Reset Value
NMI_SEL	INT_BA+0x80	R/W	NMI Interrupt Source Select Control Register	0x0000_0000

31	30	29	28	27	26	25	24
-							
23	22	21	20	19	18	17	16
-							
15	14	13	12	11	10	9	8
-							MNI_EN
7	6	5	4	3	2	1	0
-			NMI_SEL[4:0]				

Bits	Description	
[31:9]	-	Reserved.
[8]	NMI_EN	NMI Interrupt Enable 0 = IRQ0~31 assigned to NMI Disabled. (NMI still can be software triggered by setting its pending flag.) 1 = IRQ0~31 assigned to NMI Enabled.
[7:5]	-	Reserved.
[4:0]	NMI_SEL	NMI Interrupt Source Selection The NMI interrupt to Cortex-M0 can be selected from one of IRQ0~IRQ31 by setting NMI_SEL with IRQ number. The default NMI interrupt is assigned as IRQ0 interrupt if NMI is enabled by setting NMI_SEL[8].

MCU Interrupt Request Source Register (MCU_IRQ)

Register	Offset	R/W	Description	Reset Value
MCU_IRQ	INT_BA+0x84	R/W	MCU interrupt request source register	0x0000_0000

31	30	29	28	27	26	25	24
MCU_IRQ[31:24]							
23	22	21	20	19	18	17	16
MCU_IRQ[23:16]							
15	14	13	12	11	10	9	8
MCU_IRQ[15:8]							
7	6	5	4	3	2	1	0
MCU_IRQ[7:0]							

Bits	Description
[31:0]	<p>MCU_IRQ Source Register</p> <p>The MCU_IRQ collects all the interrupts from the peripherals and generates the synchronous interrupt to Cortex-M0.</p> <p>The MCU_IRQ collects all interrupts from each peripheral and synchronizes them and then interrupts the Cortex-M0.</p> <p>When the MCU_IRQ[n] is 0:</p> <p>1 = Generate an interrupt to Cortex_M0 NVIC[n].</p> <p>0 = No effect.</p> <p>When the MCU_IRQ[n] is 1 (means an interrupt is assert):</p> <p>1 = Clear the interrupt and MCU_IRQ[n].</p> <p>0 = No effect.</p>



MCU Interrupt Request Control Register (MCU_IRQCR)

Register	Offset	R/W	Description	Reset Value
MCU_IRQCR	INT_BA+0x88	R/W	MCU Interrupt Request Control Register	0x0000_0000

31	30	29	28	27	26	25	24
23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
							FAST_IRQ

Bits	Description
[31:1]	- Reserved.
[0]	FAST_IRQ Fast IRQ Latency Enable 1= MCU IRQ latency will not fixed, MCU will enter IRQ handler as soon as possible when interrupt happened. 0= MCU IRQ latency is fixed at 13 HCLK, MCU will enter IRQ handler after this fixed latency when interrupt happened.

8 CLOCK CONTROL

8.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex™-M0 core executes the WFI instruction only if the SLEEPDEEP (SCR[2]) bit are both set to 1.. After that, chip enter Power-down mode and wait for waking-up interrupt source triggered to leave power-down mode. In the Power-down mode, the clock controller turns off the external 4~24 MHz high speed crystal and internal 22.1184 MHz high speed oscillator to reduce the overall system power consumption.

8.2 Clock Generator

The clock generator consists of 4 clock sources which are listed below:

- External 4~24 MHz high speed crystal.
- Internal 22.1184 MHz high speed oscillator.
- Programmable PLL output. (PLL source consists of external 4~24 MHz high speed crystal and internal 22.1184 MHz high speed oscillator.)
- Internal 10 kHz low speed oscillator.

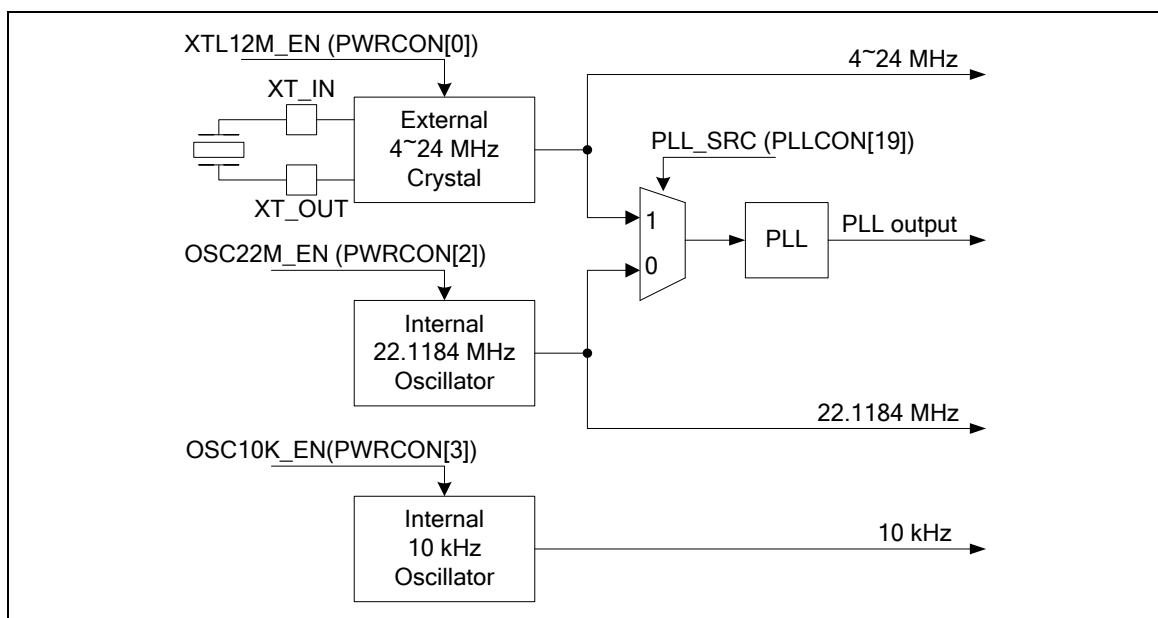


Figure 8-1 Clock Generator Block Diagram

8.3 System Clock & SysTick Clock

The system clock has 4 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is showed in Figure 8–2.

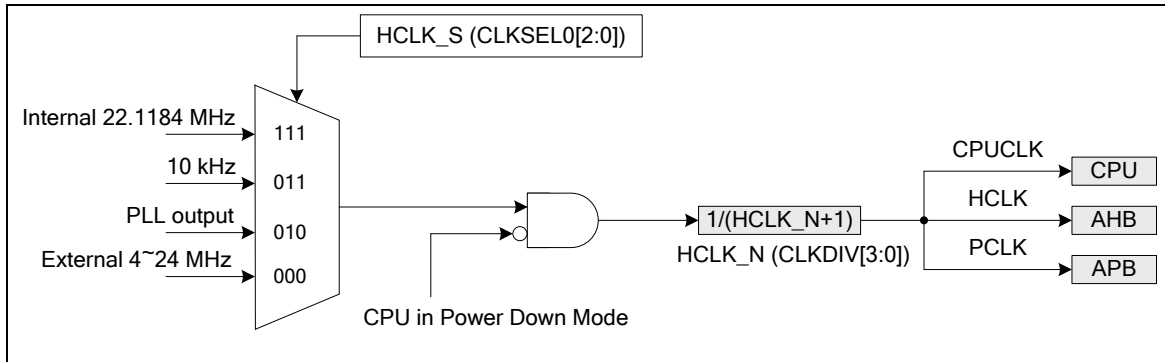


Figure 8–2 System Clock Block Diagram

The clock source of SysTick clock (STCLK) in Cortex-M0 core comes from 4 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is showed in Figure 8–3.

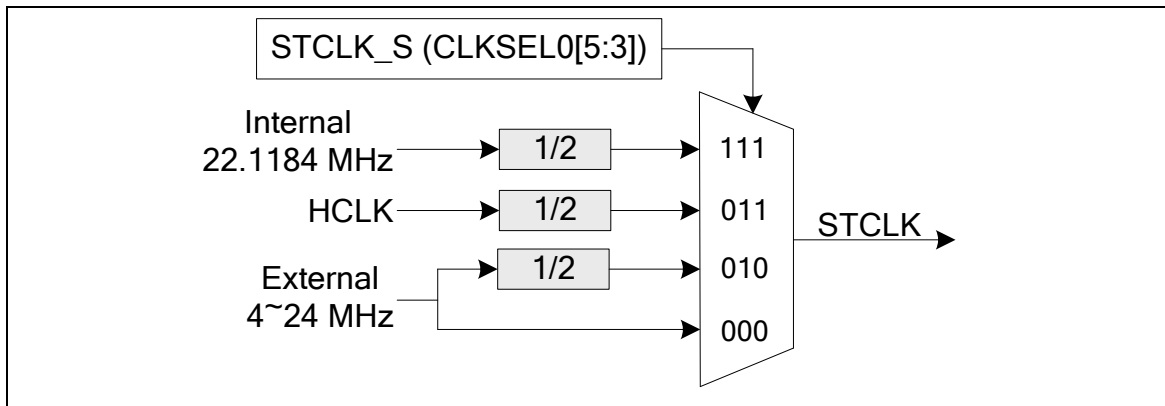


Figure 8–3 SysTick Clock Control Block Diagram

8.4 Peripherals Clock

The peripherals clock had different clock source switch setting which depends on the different peripheral. Please refer the CLKSEL1 and CLKSEL2 register description in 5.3.7.

8.5 Power-down mode (Deep Sleep Mode) Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clock are still active in Power-down mode.

Clocks and peripherals which still keep active:

- Clock Generator
 - ◆ Internal 10 kHz oscillator clock.
- Peripherals Clock (when these IP adopt 10 kHz as clock source)
 - ◆ Watchdog Timer.

8.6 Frequency Divider Output

This device is equipped a frequency divider which is composed by 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of divided clocks.

The output formula is $F_{CLKO} = F_{FRQDIV_CLK} / 2^{(N+1)}$, where F_{FRQDIV_CLK} is the input clock frequency, F_{CLKO} is the clock divider output frequency and N is the 4-bit value in FSEL (FRQDIV[3:0]).

When write 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When write 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

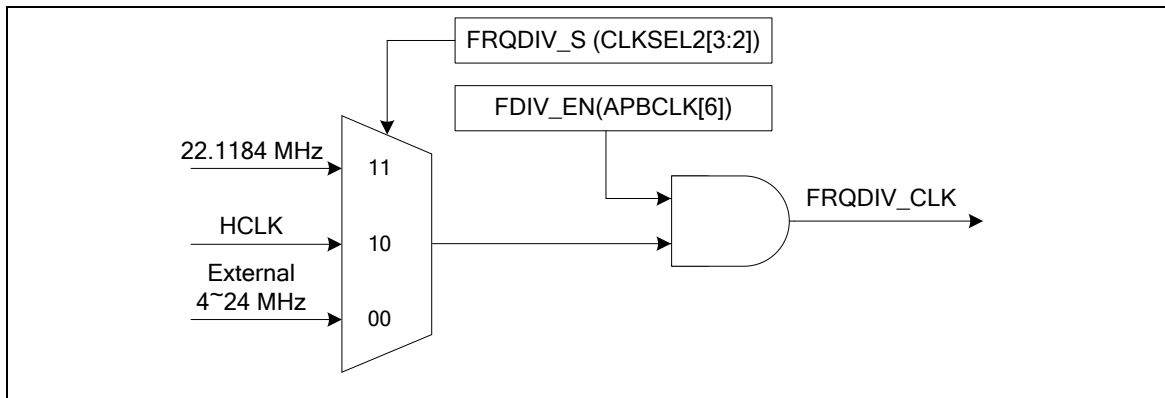


Figure 8-4 Clock Source of Frequency Divider

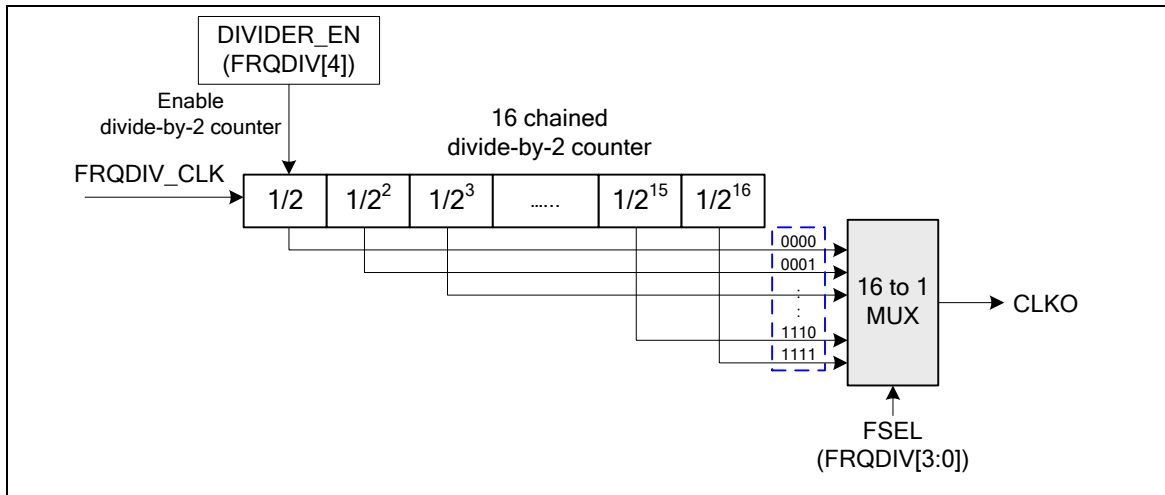


Figure 8-5 Block Diagram of Frequency Divider

9 GENERAL PURPOSE I/O

9.1 Overview

The NuMicro™ NM15xx Series has up to 82 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 82 pins are arranged in 10 ports named as P0, P1, P2, P3, P4, P5, P6, P7, P8, P9 and PA. The P0/1/2/3/4/5/6/7/8/9 port has the maximum of 8 pins and PA port has the maximum of 2 pins. Each of the 82 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as input, output, open-drain or Quasi-bidirectional mode. After reset, the I/O mode of all pins are stay at input mode. In Quasi-bidirectional mode, I/O pin has a very weak individual pull-up resistor which is about 110~300 K Ω for V_{DD} is from 5.0 V to 2.5 V.

9.2 Features

- Four I/O modes:
 - ◆ Quasi-bidirectional
 - ◆ Push-Pull output
 - ◆ Open-Drain output
 - ◆ Input only with high impedance
- TTL/Schmitt trigger input selectable
- I/O pin configured as interrupt source with edge/level setting
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling pin interrupt function will also enable the pin wake-up function

9.3 Functional Description

9.3.1 Input Only Mode

Setting PMDm[1:0] in Pn_PMD to 00b as the Pn[m] pin is in Input mode and the I/O pin is in tri-state (high impedance) without output drive capability. The Pn_PIN value reflects the status of the corresponding port pins.

9.3.2 Push-Pull Output Mode

Setting PMDm[1:0] in Pn_PMD to 01b as the Pn[m] pin is in Push-pull Output mode and the I/O pin supports digital output function with source/sink current capability. The bit value of Pn_DOUT[m] is driven on the pin.

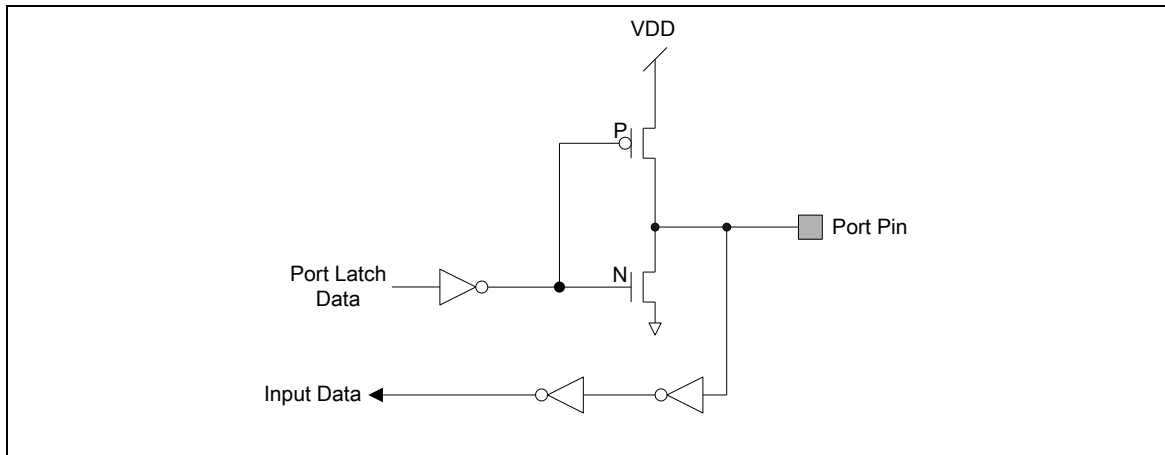


Figure 9–1 Push-Pull Output

9.3.3 Open-Drain Mode

Setting PMDm[1:0] in Pn_PMD to 10b as the Pn[m] pin is in Open-drain mode and the digital output function of I/O pin supports only sink current capability, an additional pull-up resistor is needed for driving high state. If the bit value of Pn_DOUT[m] is 0, the pin drive a “low” output on the pin. If the bit value of Pn_DOUT[m] is 1, the pin output drives high that is controlled by external pull high resistor.

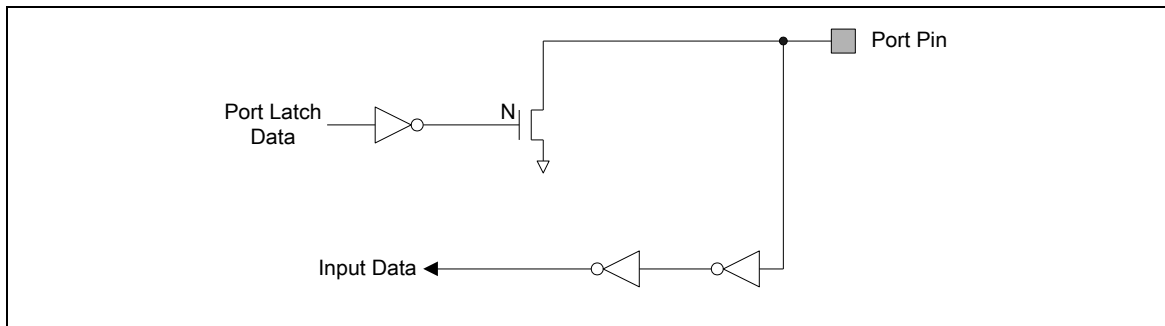


Figure 9–2 Open-Drain Output

9.3.4 Quasi Bi-directional Mode

Setting PMDm[1:0] in Pn_PMD to 11b as the Pn[m] pin is in Quasi-bidirectional mode and the I/O pin supports digital output and input function at the same time but the source current is only up to hundreds uA. Before the digital input function is performed, value of Pn_DOUT[m] must be set to 1. The quasi-bidirectional output is common on the 80C51 and most of its derivatives. If the bit value of Pn_DOUT[m] is 0, the pin drive a “low” output on the pin. If the bit value of Pn_DOUT[m] is 1, the pin will check the pin value. If pin value is high, no action takes. If pin state is low, then pin will drive strong high with 2 clock cycles on the pin and then disable the strong output drive and then the pin status is control by internal pull-up resistor. Note that the source current capability in quasi-bidirectional mode is only about 200uA to 30uA if VDD is from 5.0V to 2.5V.

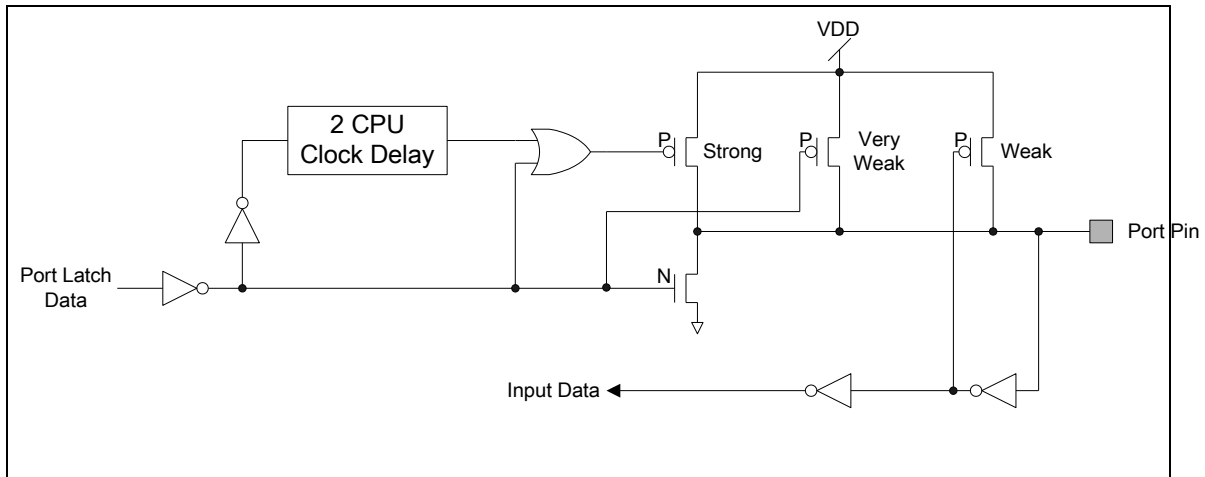


Figure 9–3 Quasi bi-directional I/O Mode

10 TIMERS/COUNTERS

10.1 Overview

The timer controller includes four 32-bit timers, TIMER0~TIMER3, which allows user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, event counting, interval measurement, clock generation, and delay timing. The timer can generate an interrupt signal upon timeout, or provide the current value during operation.

10.2 Features

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Time out period = (Period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = $(1 / T \text{ MHz}) * (2^8) * (2^{24})$, T is the period of timer clock
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Supports event counting function to count the event from external pin
- Supports external pin capture function for interval measurement
- Supports external pin capture function for reset timer counter.

11 WATCHDOG TIMER (WDT)

11.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

11.2 Features

- 18-bit free running up counter for Watchdog Timer time out interval.
- Selectable time out interval ($2^4 \sim 2^{18}$) and the time out interval is 104 ms ~ 26.3168 s (if WDT_CLK = 10 kHz).
- System keep in reset state for a period of $(1 / \text{WDT_CLK}) * 63$
- Supports selectable Watchdog Timer reset delay period, it includes $(1024+2)$ 、 $(128+2)$ 、 $(16+2)$ or $(1+2)$ WDT_CLK reset delay period.
- Supports force Watchdog Timer enabled after chip powered on or reset while CWDTEN (Config0[31] watchdog enable) bit is set to 0.
- Supports Watchdog Timer time out wake-up function when WDT clock source is selected to 10 kHz low speed oscillator

12 WINDOW WATCHDOG TIMER (WWDT)

12.1 Overview

The purpose of Window Watchdog Timer is to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

12.2 Features

- 6-bit down counter (WWDTVAL[5:0]) and 6-bit compare value (WWDTCCR[21:16] – WINCMP value) to make the window period flexible
- Selectable maximum 11-bit WWDT clock pre-scale (WWDTCCR[11:8] – PERIODSEL value) to make WWDT time out interval variable

13 BASIC PWM GENERATOR AND CAPTURE TIMER (BPWM)

13.1 Overview

The NuMicro™ NM15xx series has 1 sets of BPWM group supporting 1 sets of PWM generators that can be configured as 2 independent PWM outputs, PWM20~PWM21, or as 1 complementary PWM pairs, (PWM20, PWM21) with programmable Dead-zone generators.

The PWM generator has one 8-bit pre-scalar, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM down-counters for PWM period control, two 16-bit comparators for PWM duty control and one dead-zone generator. The PWM generator provides two independent PWM interrupt flags which are set by hardware when the corresponding PWM period down counter reaches zero. Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When PCR.DZEN01 is set, PWM20 and PWM21 perform complementary; the paired PWM timing, period, duty and dead-time are determined by PWM0 timer and Dead-zone generator 0.

To prevent PWM driving output pin from glitches, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers the updated value will be load into the 16-bit down counter/ comparator at the time down counter reaching zero. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches zero, the interrupt request is generated. If PWM-timer is set as auto-reload mode, when the down counter reaches zero, it is reloaded with PWM Counter Register (CNRx) automatically then start decreasing, repeatedly. If the PWM-timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches zero.

The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

The alternate feature of the PWM timer is digital input capture function. If capture function is enabled the PWM output pin is switched as capture input mode. The capture20 and PWM20 share one timer which is included in PWM20; and the capture21 and PWM21 share PWM21 timer, and etc. Therefore user must set the PWM timer before enable capture feature. After capture feature is enabled, the capture always latched PWM counter to Capture Rising Latch Register (CRLR) when input channel has a rising transition and latched PWM-counter to Capture Falling Latch Register (CFLR) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CCR.CRL_IE0[1] (Rising latch Interrupt enable) and CCR.CFL_IE0[2] (Falling latch Interrupt enable) to decide the condition of interrupt occur. Capture channel 1 has the same feature by setting CCR.CRL_IE1[17] and CCR.CFL_IE1[18].

The maximum captured frequency that PWM can capture is confined by the capture interrupt latency. When capture interrupt occurred, software will do at least three steps, they are: Read PIIR to get interrupt source and Read PWM_CRLx/PWM_CFLx(x=0~1) to get capture value and finally write 1 to clear PIIR to zero. If interrupt latency will take time T0 to finish, the capture signal mustn't transition during this interval (T0). In this case, the maximum capture frequency will be 1/T0. For example:

HCLK = 50MHz, BPWM_CLK = 25MHz, Interrupt latency is 900 ns

So the maximum capture frequency will is 1/900ns ≈ 1000 kHz

13.2 Features

13.2.1 PWM Function:

- One PWM generator which supports one 8-bit pre-scalar, one clock divider, two PWM timers (down counter), one dead-zone generator and two PWM outputs.
- Up to 16-bit resolution
- PWM Interrupt request synchronized with PWM period
- One-shot or Auto-reload mode PWM
- Edge-aligned type or Center-aligned type option

13.2.2 Capture Function:

- Timing control logic shared with PWM generators
- Supports 2 Capture input channels shared with 2 PWM output channels
- Each channel supports one rising latch register (CRLR), one falling latch register (CFLR) and Capture interrupt flag (CAPIFx)

14 ENHANCED PWM GENERATOR FOR MOTOR DRIVE (EPWM)

14.1 Overview

This device has two built-in PWM units with the same architecture whose function is specially designed for driving motor control applications. Using the PWM, input capture module and QEI controller with proper control flow by software can easily drive the 3-phase Brushless DC motor, 3-phase AC induction motor, and DC motor.

14.2 Features

Each unit supports the features listed below:

- **Three** independent 16-bit PWM duty control units with maximum 6 port pins:
 - **Three independent PWM output:**
PWM00, PWM02 and PWM04 for Unit 0
PWM10, PWM12 and PWM14 for Unit 1
 - **Three complementary PWM pairs**, with each pin in a pair mutually complement to each other and capable of programmable dead-time insertion:
(PWMx0,PWMx1), (PWMx2,PWMx3) and (PWMx4,PWMx5) where x=0~1.
 - 3 synchronous PWM pairs, with each pin in a pair in-phase:
(PWM0,PWM1), (PWM2,PWM3) and (PWM4,PWM5)
- Group control bit:
PWM2 and PWM4 are synchronized with PWM0
- Supports Edge-aligned mode and Center-aligned mode
- Programmable dead-time insertion between complementary paired PWMs
- Each pin of from PWM0 to PWM5 has independent polarity setting control
- Mask output control for Electrically Commutated Motor operation
- Tri-state output at reset and brake state
- Hardware brake protections.
- Two Interrupt Sources:
 - Interrupt is synchronously requested at PWM frequency when up/down counter comparison matched (Edge- and Center-aligned modes) or underflow (Center-aligned mode).
 - Interrupt is requested when external brake pins asserted
- The PWM signals before polarity control stage are defined in view of positive logic. The PWM ports is active high or active low are controlled by polarity control register.
- High Source/Sink current

After CPU reset, the internal output of the each PWM channels depends on the polarity setting. The interval between successive outputs is controlled by a 16-bit up/down counter which uses a software selectable clock source with configurable internal clock pre-scalar as its input. The PWM counter clock has the frequency as the clock source $F_{PWM} = EPWMx_CLK/Pre\text{-}scalar$; Here the EPWMx_CLK synchronized with CPU clock HCLK.

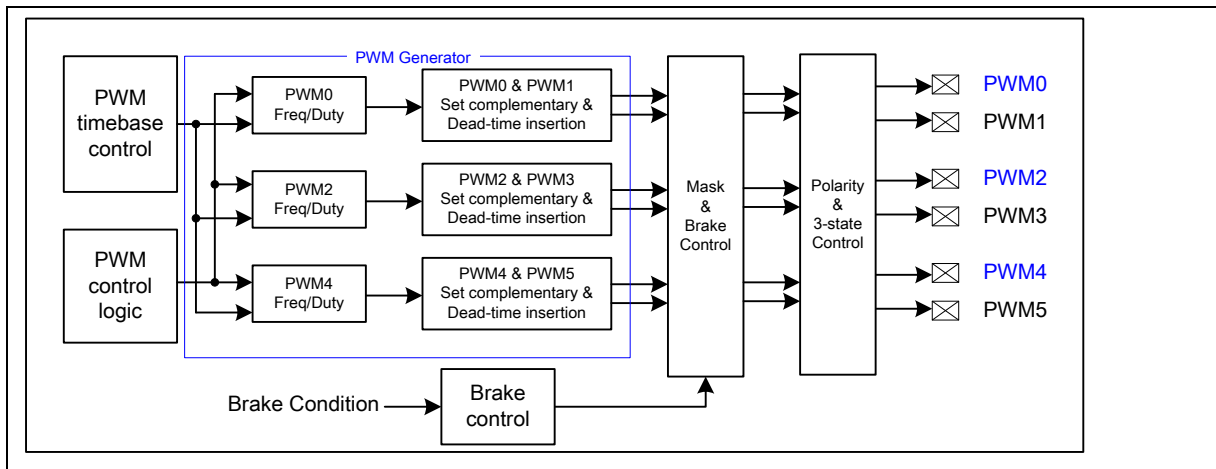


Figure 14-1 PWM Block Diagram

15 MOTOR DRIVE UNIT (MDU)

15.1 Overview

An efficient motor control scheme, Field Orientated Control (FOC), is widely applied to a three phases AC Induction Motor (ACIM) and Permanent Magnet Synchronous Motor (PMSM). This device provides a motor drive unit (MDU) which performs the Field Orientated Control (FOC) through hardware and offers the Space Vector PWM duty timing to PWM unit0 to produce the PWM signals to power inverter.

15.2 Features

- Clarke and Inverse Clarke Transformation
- Park and Inverse Park Transformation
- Two built-in PI (Proportional and Integral) controllers
- Space-vector PWM (SVPWM) timing generator
- Arithmetic operation in fixed point Q-15 format
- Auto update PWM Unit0 duty registers

16 HARDWARE DIVIDER

16.1 Overview

The hardware divider is useful to the high performance application. The hardware divider is a signed, integer divider with both quotient and remainder outputs.

16.2 Features

- Signed (two's complement) integer calculation.
- 32-bit dividend with 16-bit divisor calculation capacity.
- Both 32-bit quotient and 16-bit remainder outputs.
- Divided by 0 warning flag.
- 7 HCLK clocks taken for one cycle calculation.
- Software triggered with finish flag.
- Triggered by MDU under background automatically.

17 ENHANCED INPUT CAPTURE TIMER

17.1 Overview

This device provides up to two units of Input Capture Timer/Counter which capture function can detect the digital edge changed signal at channel inputs. Each unit has three input capture channels. The timer/counter is equipped with up counting, reload and compare-match capabilities.

17.2 Features

- Up to two Input Capture Timer/Counter Units, Input Capture 0 and Input Capture 1.
- Each unit has own interrupt vector
- 24-bit Input Capture up-counting timer/counter
- With noise filter in front end of input ports
- Edge detector with three options
 - Rising edge detection
 - Falling edge detection
 - Both edge detection
- Each input channel is supported with one capture counter hold register
- Captured event reset/reload capture counter option
- Supports the compare-match function

18 QUADRATURE ENCODER INTERFACE (QEI)

18.1 Overview

There are two QEI controllers in this device. The Quadrature Encoder Interface (QEI) decodes speed of rotation and motion sensor information. It can be used in any application that uses a quadrature encoder for feedback.

18.2 Features

- Up to two QEI controllers, QEI0 and QEI1.
- Two QEI phase inputs, QEA and QEB; One Index input.
- One QEI control register (QEI_CTR) and one QEI Status Register (QEI_STS)
- Four Quadrature encoder pulse counter operation modes
 - Mode0: x4 free-counting mode
 - Mode1: x2 free-counting mode
 - Mode2: x4 compare-counting mode
 - Mode3: x2 compare-counting mode
- Encoder Pulse Width measurement mode

19 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

19.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function, LIN master/slave mode function and RS-485 mode functions. Each UART channel supports seven types of interrupts including

- Transmitter FIFO empty interrupt (INT_THRE)
- Receiver threshold level reached interrupt (INT_RDA),
- Line status interrupt (parity error or frame error or break interrupt) (INT_RLS),
- Receiver buffer time out interrupt (INT_TOUT),
- MODEM/Wake-up status interrupt (INT_MODEM),
- Buffer error interrupt (INT_BUF_ERR)
- LIN interrupt (INT_LIN)

The UART controller is built-in with a 16-byte transmitter FIFO (TX_FIFO) and a 16-byte receiver FIFO (RX_FIFO) that reduces the number of interrupts presented to the CPU. The CPU can read the status of the UART at any time during the operation. The reported status information includes the type and condition of the transfer operations being performed by the UART, as well as 4 error conditions (parity error, frame error, break interrupt and buffer error) probably occur while receiving data. The UART includes a programmable baud rate generator that is capable of dividing clock input by divisors to produce the serial clock that transmitter and receiver need. The baud rate equation is $\text{Baud Rate} = \text{UART_CLK} / M * [\text{BRD} + 2]$, where M and BRD are defined in Baud Rate Divider Register (UA_BAUD). Table 19-1 lists the equations in the various conditions and Table 19-2 lists the UART baud rate setting table.

Mode	DIV_X_EN	DIV_X_ONE	Divider X	BRD	Baud Rate Equation
0	0	0	Don't care	A	$\text{UART_CLK} / [16 * (A+2)]$
1	1	0	B	A	$\text{UART_CLK} / [(B+1) * (A+2)]$, B must ≥ 8
2	1	1	Don't care	A	$\text{UART_CLK} / (A+2)$, A must ≥ 3

Table 19-1 UART Baud Rate Equation

System clock = internal 22.1184 MHz high speed oscillator						
Baud Rate	Mode 0		Mode 1		Mode 2	
	Parameter	Register	Parameter	Register	Parameter	Register
921600	x	x	A=0,B=11	0x2B00_0000	A=22	0x3000_0016
460800	A=1	0x0000_0001	A=1,B=15 A=2,B=11	0x2F00_0001 0x2B00_0002	A=46	0x3000_002E
230400	A=4	0x0000_0004	A=4,B=15 A=6,B=11	0x2F00_0004 0x2B00_0006	A=94	0x3000_005E

115200	A=10	0x0000_000A	A=10,B=15 A=14,B=11	0x2F00_000A 0x2B00_000E	A=190	0x3000_00BE
57600	A=22	0x0000_0016	A=22,B=15 A=30,B=11	0x2F00_0016 0x2B00_001E	A=382	0x3000_017E
38400	A=34	0x0000_0022	A=62,B=8 A=46,B=11 A=34,B=15	0x2800_003E 0x2B00_002E 0x2F00_0022	A=574	0x3000_023E
19200	A=70	0x0000_0046	A=126,B=8 A=94,B=11 A=70,B=15	0x2800_007E 0x2B00_005E 0x2F00_0046	A=1150	0x3000_047E
9600	A=142	0x0000_008E	A=254,B=8 A=190,B=11 A=142,B=15	0x2800_00FE 0x2B00_00BE 0x2F00_008E	A=2302	0x3000_08FE
4800	A=286	0x0000_011E	A=510,B=8 A=382,B=11 A=286,B=15	0x2800_01FE 0x2B00_017E 0x2F00_011E	A=4606	0x3000_11FE

Table 19-2 UART Baud Rate Setting Table

The UART controller support auto-flow control function that uses two low-level signals, nCTS (clear-to-send) and nRTS (request-to-send), to control the flow of data transfer between the chip and external devices (ex: Modem). When auto-flow is enabled, the UART is not allowed to receive data until the UART asserts nRTS to external device. When the number of bytes in the RX FIFO equals the value of RTS_TRI_LEV (UA_FCR [19:16]), the nRTS is de-asserted. The UART sends data out when UART controller detects nCTS is asserted from external device. If a valid asserted nCTS is not detected the UART controller will not send data out.

The UART controllers also provides Serial IrDA (SIR, Serial Infrared) function (User must set IrDA_EN (UA_FUN_SEL [1]) to enable IrDA function). The SIR specification defines a short-range infrared asynchronous serial transmission mode with 1 start bit, 8 data bits, and 1 stop bit. The maximum data rate supports up to 115.2 Kbps (half duplex). The IrDA SIR block contains an IrDA SIR Protocol encoder/decoder. The IrDA SIR Protocol encoder/decoder is half-duplex only. So it cannot transmit and receive data at the same time. The IrDA SIR physical layer specifies a minimum 10ms transfer delay between transmission and reception, and this delay feature must be implemented by software.

The alternate function of UART controllers is LIN (Local Interconnect Network) function. The LIN mode is selected by setting the UA_FUN_SEL[1:0] to '01'. In LIN mode, 1 start bit and 8 data bits format with 1 stop bit are required in accordance with the LIN standard.

For the NuMicro™ NM15xx Series, another alternate function of UART controllers is RS-485 9-bit mode, and direction control provided by nRTS pin or can program GPIO (PB.2 for UART0_nRTS and PB.6 for UART1_nRTS) to implement the function by software. The RS-485 mode is selected by setting the UA_FUN_SEL register to select RS-485 function. The RS-485 transceiver control is implemented using the nRTS control signal from an asynchronous serial port to enable the RS-485 transceiver. In RS-485 mode, many characteristics of the receiving and transmitting are same as UART.

19.2 Features

- Full duplex, asynchronous communications
- Separates receive / transmit 16 bytes entry FIFO for data payloads
- Supports hardware auto flow control/flow control function (nCTS, nRTS) and programmable nRTS flow control trigger level
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports nCTS wake-up function
- Supports 7-bit receiver buffer time out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting UA_TOR [DLY] register
- Supports break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
 - Programmable data bit length, 5-, 6-, 7-, 8-bit character
 - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
 - Programmable stop bit length, 1, 1.5, or 2 stop bit generation
- IrDA SIR function mode
 - Supports 3-/16-bit duration for normal mode
- LIN function mode
 - Supports LIN master/slave mode
 - Supports programmable break generation function for transmitter
 - Supports break detect function for receiver
- RS-485 function mode
 - Supports RS-485 9-bit mode
 - Supports hardware or software direct enable control provided by nRTS pin

20 SERIAL PERIPHERAL INTERFACE (SPI)

20.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol that operates in full duplex mode. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The NuMicro™ NM15xx series contains up to three sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each set of SPI controller can be configured as a master or a slave device.

20.2 Features

- Up to three sets of SPI controller
- Supports Master or Slave mode operation
- Configurable bit length of a transfer word from 8 to 32-bit
- Provides separate 8-layer depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports the byte reorder function
- Supports Byte or Word Suspend mode
- Supports 3-wire, no slave select signal, bi-direction interface

21 I²C SERIAL INTERFACE

21.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the Figure 21-1 for more detailed I²C BUS Timing.

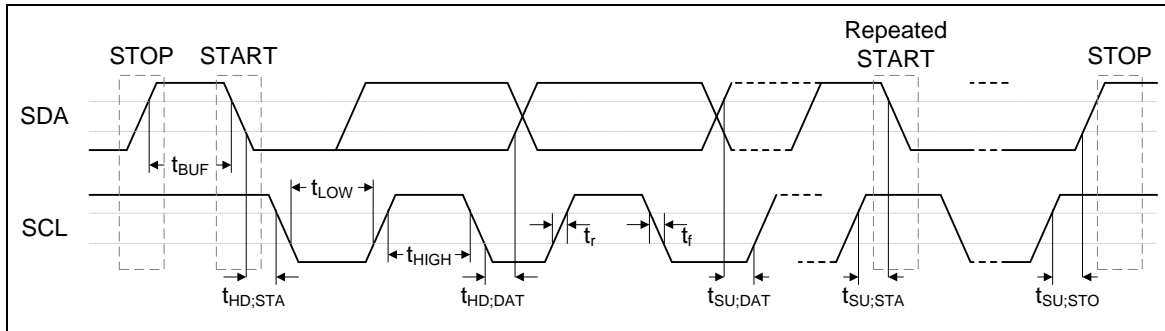


Figure 21-1 I²C Bus Timing

The device's on-chip I²C logic provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. To enable this port, the bit ENS1 in I2CON should be set to '1'. The I²C H/W interfaces to the I²C bus via two pins: SDA and SCL. Pull-up resistor is needed for I²C operation as these SDA and SCL are open drain pins. When the I/O pins are used as I²C port, user must set the pins function to I²C in advance.

21.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus are:

- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Built-in a 14-bit time out counter requested the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.
- External pull-up resistors are needed for high output
- Programmable clocks allow versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)

22 CONTROLLER AREA NETWORK (CAN)

22.1 Overview

The C_CAN consists of the CAN Core, Message RAM, Message Handler, Control Registers and Module Interface. The CAN Core performs communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1MBit/s. For the connection to the physical layer, additional transceiver hardware is required.

For communication on a CAN network, individual Message Objects are configured. The Message Objects and Identifier Masks for acceptance filtering of received messages are stored in the Message RAM. All functions concerning the handling of messages are implemented in the Message Handler. These functions include acceptance filtering, the transfer of messages between the CAN Core and the Message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the C_CAN can be accessed directly by software through the module interface. These registers are used to control/configure the CAN Core and the Message Handler and to access the Message RAM.

22.2 Features

- Supports CAN protocol version 2.0 part A and B.
- Bit rates up to 1 MBit/s.
- 32 Message Objects.
- Each Message Object has its own identifier mask.
- Programmable FIFO mode (concatenation of Message Objects).
- Maskable interrupt.
- Disabled Automatic Re-transmission mode for Time Triggered CAN applications.
- Programmable loop-back mode for self-test operation.
- 16-bit module interfaces to the AMBA APB bus.
- Supports wake-up function.

23 12-BIT ANALOG-TO-DIGITAL CONVERTER

23.1 Overview

The NuMicro™ NM15xx Series contains two 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 16 input channels. The two A/D converters ADCA and ADCB can be sampled with Simultaneous or Single Sampling mode. The A/D converters can be started by software, PWM triggers, timer0~3 overflow pulse triggers, ADINT0, ADINT1 interrupt EOC pulse trigger and external STADC pin input signal.

Note: The analog input port pins must be configured as input type before the ADC function is enabled.

23.2 Features

- Analog input voltage range: 0~Vref (Max to 5.0V).
- 12-bit resolution and 10-bit accuracy is guaranteed.
- Up to 16 single-end analog input channels.
- Two SAR ADC converters.
- Four ADC interrupts with individual interrupt vector addresses.
- Maximum ADC clock frequency is use 16MHz.
- Up to 1.6M SPS conversion rate, each of ADC converter conversion time less than 1.25μs.
- Two operating modes
 - ◆ Single sampling mode: two ADC converters run at normal operation.
 - ◆ Simultaneous sampling mode: Allow two ADC converters can be sampled simultaneously.
- An A/D conversion can be started by:
 - ◆ Writing 1 to ADSTx bit (x = 0~15) through software
 - ◆ External pin STADC
 - ◆ Timer0~3 overflow pulse triggers
 - ◆ ADINT0, ADINT1 interrupt EOC pulse triggers
 - ◆ PWM triggers
- Conversion results are held in 16 data registers with valid and overrun indicators.
- SAMPLEA0~7 ADC control logic modules, each of them is configurable for ADCA converter channel AINA0~7 and trigger source.
- SAMPLEB0~7 ADC control logic modules, each of them is configurable for ADCB converter channel AINB0~7 and trigger source.
- Channel AINA0 supports 2 input sources: external analog voltage and internal OP0 Amplifier output voltage.
- Channel AINB0 supports 2 input sources: external analog voltage and internal OP1 Amplifier output voltage.
- Channel AINA7 supports 4 input sources: external analog voltage, internal fixed band-gap voltage, internal temperature sensor output, and analog ground.

24 ANALOG COMPARATOR

24.1 Overview

The NuMicro™ NM15xx Series contains three comparators which can be used in a number of different configurations. The comparator output is logic 1 when positive input voltage is greater than negative input voltage; otherwise the output is logic 0. Each comparator can be configured to cause an interrupt when the comparator output value changes.

Note: the analog input port pins must be configured as input type before Analog Comparator function is enabled.

24.2 Features

- Analog input voltage range: 0~ V_{DDA}
- Supports Hysteresis function
- Supports optional internal reference voltage input at negative end
- Supports optional OP amplifier output voltage input at positive end
- Supports comparator output inverse function
- Supports the comparator output can be the brake source for EPWM function

25 OP AMPLIFIER

25.1 Overview

This device integrated two operational amplifiers. It can be enabled through OPx_EN bit. User can measure the outputs of the OP amplifier as the OP amplifier output to the integrated A/D converter channel AINA[0] and AINB[0], where digital results can be taken.

Note: The analog input port pins must be configured as input type before the OP amplifier function is enabled.

25.2 Features

- Analog input voltage range: 0~Vdd.
- Two analog OP amplifiers.
- Software enabled to connect OP amplifier 0,1 outputs to A/D converter channel AINA[0], AINB[0] respectively.
- Schmitt trigger buffer outputs of OP amplifier 0, 1 can be one of the comparator interrupt sources.
- OP amplifier 0 output can be an optional input source of integrated comparator 0 positive input.
- OP amplifier 1 output can be an optional input source of integrated comparator 1 positive input.

26 FLASH MEMORY CONTROL (FMC)

26.1 Overview

The NuMicro™ NM15xx Series has 128K/64K/32K bytes on-chip embedded Flash for application program memory (APROM) that can be updated through ISP procedure. The In-System-Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip is powered on, Cortex™-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, the NuMicro™ NM15xx Series also provides additional DATA Flash for user to store some application dependent data. For 128K bytes APROM device, the data flash is shared with original 128K program memory and its start address is configurable in Config1. For 64K/32K bytes APROM device, the data flash is fixed at 4K.

26.2 Features

- Runs up to 72 MHz and optional up to 50 MHz with zero wait state for continuous address read access
- All embedded flash memory supports 512 bytes page erase
- 128K/64K/32KB application program memory (APROM)
- 8 KB In-System-Programming (ISP) loader program memory (LDROM)
- 4KB data flash for 64K/32KB APROM device
- Configurable data flash size for 128KB APROM device
- Configurable or fixed 4 KB data flash with 512 bytes page erase unit
- Support In-Application-Programming (IAP) to switch code between APROM and LDROM without reset
- In-System-Programming (ISP) to update on-chip Flash

27 ELECTRICAL CHARACTERISTICS

27.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	VDD-VSS	-0.3	+6.3	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	1/t _{CLCL}	4	24	MHz
Operating Temperature	TA	-40	105	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into VDD		-	120	mA
Maximum Current out of VSS			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

27.2 DC Electrical Characteristics

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V _{DD}	2.5	-	5.5	V	V _{DD} = 2.5V ~ 5.5V
Power Ground	V _{SS} / AV _{SS}	-0.3	-	-	V	
LDO Output Voltage	V _{LDO}	1.62	1.8	1.98	V	V _{DD} ≥ 2.5V
Analog Operating Voltage	AV _{DD}	2.5	-	V _{DD}	V	
Analog Reference Voltage	V _{ref}	1.2	-	AV _{DD}	V	
Operating Current Normal Run Mode	I _{DD1}	-	-	0.61F+8.1	mA	V _{DD} = 5V, enable all IP and PLL, external XTAL
	I _{DD2}	-	-	0.32F+7.7	mA	V _{DD} = 5V, disable all IP and enable PLL, external XTAL
	I _{DD3}	-	-	0.58F+8.1	mA	V _{DD} = 3.3V, enable all IP and PLL, external XTAL
	I _{DD4}	-	-	0.29F+7.7	mA	V _{DD} = 3.3V, disable all IP and enable PLL, external XTAL
	I _{DD5}	-	-	0.66F+0.4	mA	V _{DD} = 5V, enable all IP and disable PLL, external XTAL
	I _{DD6}	-	-	0.40F+0.2	mA	V _{DD} = 5V, disable all IP and disable PLL, external XTAL
	I _{DD7}	-	-	0.60F+0.4	mA	V _{DD} = 3.3V, enable all IP and disable PLL, external XTAL
	I _{DD8}	-	-	0.35F+0.2	mA	V _{DD} = 3.3V disable all IP and disable PLL, external XTAL

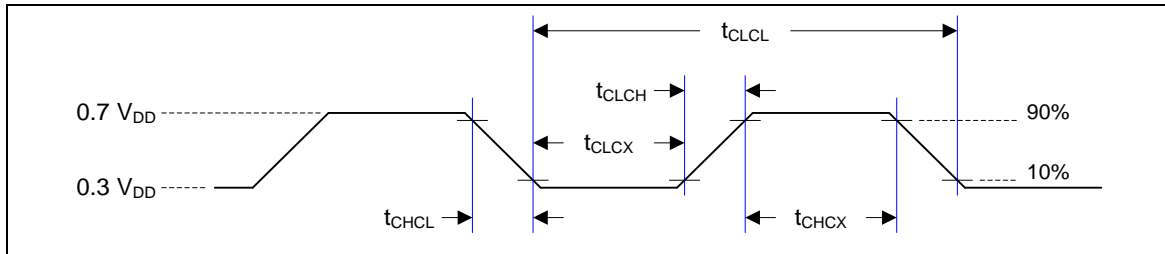
PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Current Idle Mode	I _{IDLE1}	-	-	0.39F+8.1	mA	V _{DD} = 5V, enable all IP and PLL, external XTAL
	I _{IDLE2}	-	-	0.09F+7.7	mA	V _{DD} = 5V, disable all IP and enable PLL, external XTAL
	I _{IDLE3}	-	-	0.37F+8.1	mA	V _{DD} = 3.3V, enable all IP and PLL, external XTAL
	I _{IDLE4}	-	-	0.08F+7.7	mA	V _{DD} = 3.3V, disable all IP and enable PLL, external XTAL
	I _{IDLE5}	-	-	0.43F+0.5	mA	V _{DD} = 5V, enable all IP and disable PLL, external XTAL
	I _{IDLE6}	-	-	0.18F+0.4	mA	V _{DD} = 5V, disable all IP and disable PLL, external XTAL
	I _{IDLE7}	-	-	0.38F+0.5	mA	V _{DD} = 3.3V, enable all IP and disable PLL, external XTAL
	I _{IDLE8}	-	-	0.13F+0.4	mA	V _{DD} = 3.3V disable all IP and disable PLL, external XTAL
Standby Current Power-down Mode	I _{PWD}	-	-	25	μA	V _{DD} = 5.5V, No load @ Disable BOV function, 25°C
Logic 0 Input Current (Quasi-bidirectional mode)	I _{IL}	-	-	-75	μA	
Input Leakage Current (input only)	I _{LK}	-	-	2	μA	
Logic 1 to 0 Transition Current (Quasi-bidirectional mode)	I _{TL} ^[3]	-	-	-660	μA	V _{DD} = 5.5V, V _{IN} < 2.0V
Internal Pull-High Resistor of /RESET ^[1]	R _{RST}	15	-	-	kΩ	

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Input Low Voltage (TTL input)	V_{IL}	-0.3	-	$0.2V_{DD}-0.1$	V	
Input Low Voltage (Schmitt input)	V_{IL1}	-0.3		$0.3V_{DD}$	V	
Input Low Voltage (/RESET, XTAL in)	V_{IL2}	-0.3		$0.15V_{DD}$	V	
Input High Voltage (TTL input)	V_{IH}	$0.2V_{DD}+0.9$	-	$V_{DD}+0.3$	V	
Input High Voltage (Schmitt input, /RESET, XTAL in)	V_{IH1}	$0.7V_{DD}$	-	$V_{DD}+0.3$	V	
Hysteresis voltage of (Schmitt input)	V_{HY}	-	$0.2V_{DD}$	-	V	
Source Current (Quasi-bidirectional Mode)	I_{OH}	-360	-	-	μA	$V_{DD} = 4.5V, V_S = 2.4V$
		-60	-	-	μA	$V_{DD} = 2.7V, V_S = 2.2V$
		-50	-	-	μA	$V_{DD} = 2.5V, V_S = 2.0V$
Source Current (Push-pull Mode)	I_{OH1}	-25	-	-	mA	$V_{DD} = 4.5V, V_S = 2.4V$
		-4	-	-	mA	$V_{DD} = 2.7V, V_S = 2.2V$
		-3	-	-	mA	$V_{DD} = 2.5V, V_S = 2.0V$
Sink Current (Quasi-bidirectional and Push-pull Mode)	I_{OL}	16	-	-	mA	$V_{DD} = 4.5V, V_S = 0.45V$
		10	-	-	mA	$V_{DD} = 2.7V, V_S = 0.45V$
		9	-	-	mA	$V_{DD} = 2.5V, V_S = 0.45V$

Note:

1. /RESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. I/O pin can source a transition current when they are being externally driven from 1 to 0. In the condition of $V_{DD}=5.5V$, 5he transition current reaches its maximum value when V_{IN} approximates to 2V.

27.3 AC Electrical Characteristics



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t _{CHCX}	Clock High Time		10	-	-	nS
t _{CLCX}	Clock Low Time		10	-	-	nS
t _{CLCH}	Clock Rise Time		2	-	15	nS
t _{CHCL}	Clock Fall Time		2	-	15	nS

27.3.1 External 4~24MHz Crystal

PARAMETER	CONDITION	MIN.	TYP..	MAX.	UNIT
Operation Voltage V _{DD}	-	2.5	-	5.5	V
Temperature	-	-40	-	85	°C
Operating Current	12 MHz at V _{DD} = 5V	-	1	-	mA
Clock Frequency	External crystal	4		24	MHz

27.3.1.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	10~20 pF	10~20 pF	without

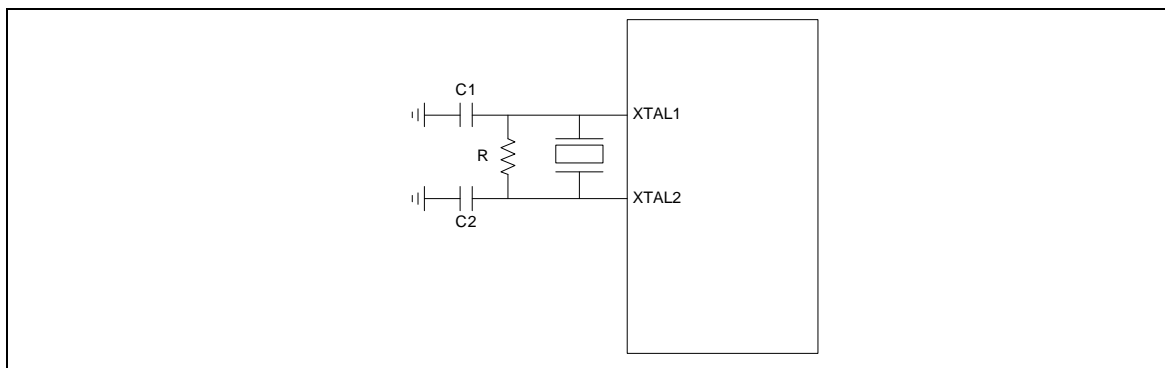


Figure 27–1 Typical Crystal Application Circuit



27.3.2 Internal 22.1184 MHz Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage	-	2.5	-	5.5	V
Frequency (After calibration)	-	-	22.1184	-	MHz
	+25°C; $V_{DD} = 5V$	-1	-	+1	%
	-40 to +105°C; $V_{DD} = 2.5V \sim 5.5V$	-2	-	+2	%
Operation Current	$V_{DD} = 5V$	-	500	-	uA

27.3.3 Internal 10 kHz Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25°C; $V_{DD} = 5V$	-30	-	+30	%
	-40°C ~ +85°C; $V_{DD} = 2.5V \sim 5.5V$	-50	-	+50	%

27.4 Analog Characteristics

27.4.1 Specification of 12-bit SARADC

PARAMETER	SYMBOL	CONDITON	MIN.	TYP.	MAX.	UNIT
Resolution	-		12			Bit
Differential nonlinearity error	DNL		-	-1~+2	-1~+4	LSB
Integral nonlinearity error	INL		-	±1.5	±4	LSB
Offset error	EO		-	+3	+5	LSB
Full scale error	EG		-	-3	-6	LSB
Absolute error	EA			-	±4	
Monotonic	-		Guaranteed			
ADC clock frequency	F_{ADC}	AVDD = 4.5V	-	-	16	MHz
		AVDD = 2.5V	-	-	8	
Sample rate	F_S	AVDD = 4.5V	-	-	800	ksps
		AVDD = 2.5V	-	-	400	
Sample time	T_S		-	8	-	Clock
Conversion time	T_{ADC}		-	12	-	Clock
Supply voltage	AVDD		2.5	-	5.5	V
VRFE voltage	VREF		2.0		AVDD	
Supply current	I_{DDA}		-	1.5	-	mA
Reference current	I_{RFE}		-	1	-	mA
Input voltage	V_{IN}		0	-	VREF	V
Resistance	R_{IN}			6		kΩ
Capacitance	C_{IN}		-	5	-	pF

27.4.2 Specification of LDO

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Input Voltage V_{DD}	2.5		5.5	V	V_{DD} input voltage
Output Voltage	1.62	1.8	1.98	V	$V_{DD} > 2.5\text{ V}$
Operating Temperature	-40	25	105	°C	
Cbp	-	1	-	μF	$R_{ESR} = 1\ \Omega$

Note:

1. It is recommended that a 10 μF or higher capacitor and a 100 nF bypass capacitor are connected between V_{DD} and the closest V_{SS} pin of the device.
2. To ensure power stability, a 1 μF or higher capacitor must be connected between LDO_CAP pin and the closest V_{SS}

pin of the device.

27.4.3 Specification of Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage	-	0	-	5.5	V
Quiescent Current	$AV_{DD}=5.5\text{ V}$	-	1	5	μA
Operation Temperature	-	-40	25	105	$^{\circ}\text{C}$
Threshold Voltage	-	1.6	2.0	2.4	V
Hysteresis	-	0	0	0	V

27.4.4 Specification of Brown-out Detector

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage	-	0	-	5.5	V
Temperature	-	-40	25	105	$^{\circ}\text{C}$
Quiescent Current	$AV_{DD}=5.5\text{ V}$	-	-	125	μA
Brown-out Voltage	BOD_VL[1:0]=11	4.2	4.4	4.6	V
	BOD_VL [1:0]=10	3.5	3.7	3.9	V
	BOD_VL [1:0]=01	2.6	2.7	2.8	V
	BOD_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

27.4.5 Specification of Power-On Reset (5V)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Temperature	-	-40	25	105	$^{\circ}\text{C}$
Reset Voltage	V+	-	2	-	V
Quiescent Current	$V_{in} > \text{reset voltage}$	-	1	-	nA

27.4.6 Specification of Temperature Sensor

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operation Voltage ^[1]		2.5	-	5.5	V
Operation Temperature		-40	-	105	°C
Current Consumption		6.4	-	10.5	μA
Gain			-1.76		mV/°C
Offset Voltage	Temp=0 °C		720		mV

27.4.7 Specification of Comparator

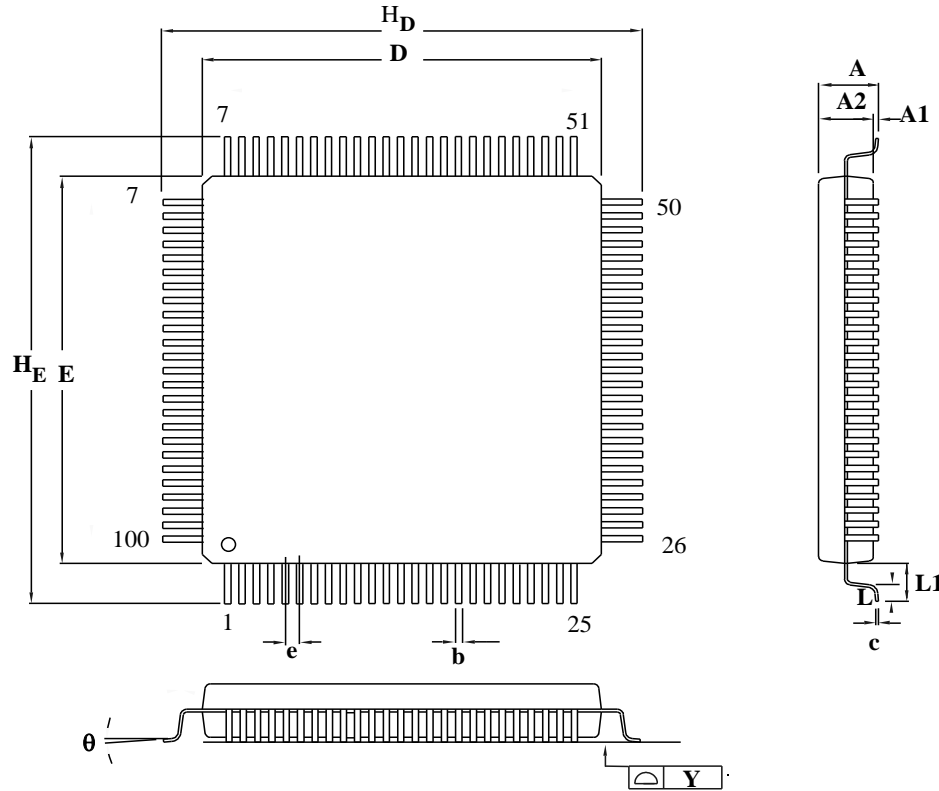
PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage AV _{DD}	-	2.5		5.5	V
Operation Temperature	-	-40	25	85	°C
Operation Current	V _{DD} =3.0 V	-	20	40	μA
Input Offset Voltage	-	-	5	15	mV
Output Swing	-	0.1	-	V _{DD} -0.1	V
Input Common Mode Range	-	0.1	-	V _{DD} -1.2	V
DC Gain	-	-	70	-	dB
Propagation Delay	VCM=1.2 V and VDIFF=0.1 V	-	200	-	ns
Comparison Voltage	20 mV at VCM=1 V 50 mV at VCM=0.1 V 50 mV at VCM=V _{DD} -1.2 10 mV for non-hysteresis	10	20	-	mV
Hysteresis	VCM=0.4 V ~ V _{DD} -1.2 V	-	±10	-	mV
Wake-up Time	CINP=1.3 V CINN=1.2 V	-	-	2	μs

27.4.8 Specification of OP Amplifier

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
AVDD	-	3.0	3.3	5.5	V
Input offset voltage	-	-	2	5	mV
Input offset average drift	-	-	-	1	uV/°C
Output swing	-	0.1	-	VDD-0.1	V
Input common mode range	-	0.1	-	VDD-1.2	V
DC gain	-	-	80	-	dB
Unity gain freq.	AVDD=5V	-	-	5	MHz
Phase margin	-	-	50°	-	°
PSRR+	AVDD=5V	-	90	-	dB
CMRR	AVDD=5V	-	90	-	dB
Slew rate	AVDD=5V, RLOAD=33K, CLOAD=50p	6.0	-	-	V/us
Wake up time	-	-	-	1	us
Quiescent current	-	-	-	2	mA

28 PACKAGE DIMENSIONS

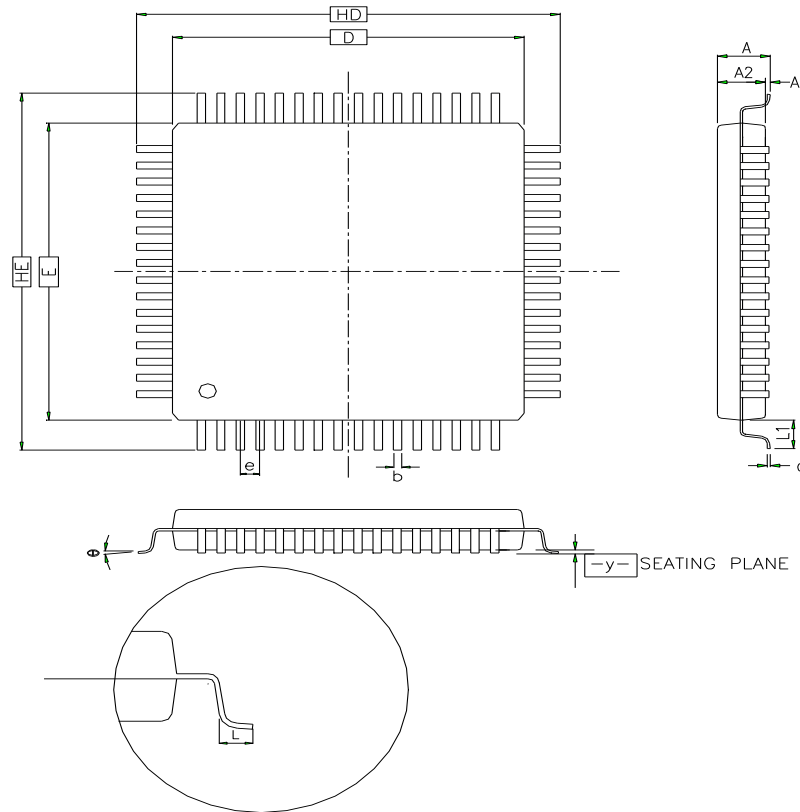
28.1 100L LQFP (14x14x1.4 mm footprint 2.0mm)



Controlling Dimension : Millimeters

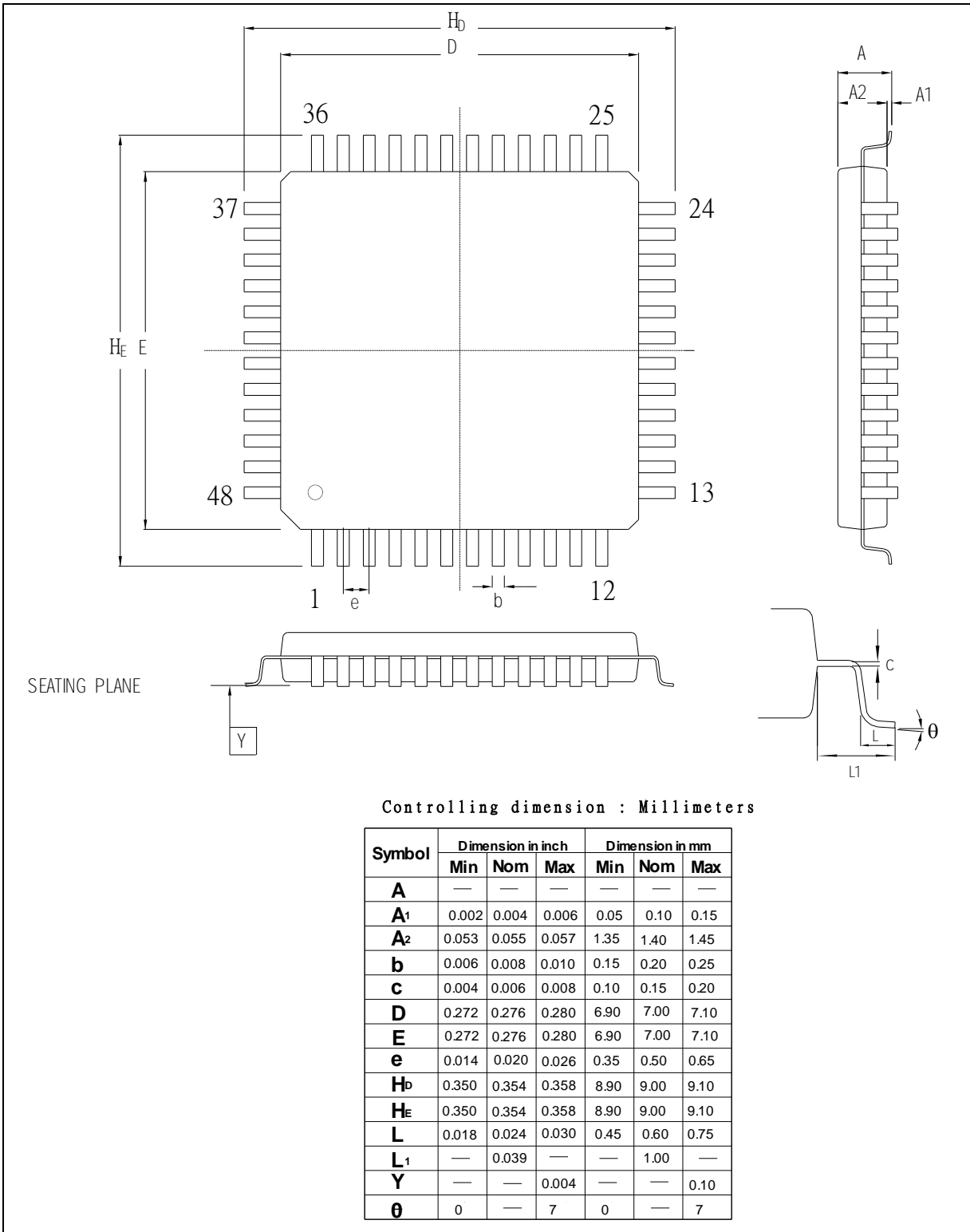
Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	—	—	0.05	—	—
A	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.556	13.90	14.00	14.10
E	0.547	0.551	0.556	13.90	14.00	14.10
e	—	0.020	—	—	0.50	—
H_D	0.622	0.630	0.638	15.80	16.00	16.20
H_E	0.622	0.630	0.638	15.80	16.00	16.20
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

28.2 64L LQFP (10x10x1.4mm footprint 2.0 mm)



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A₁	0.002	—	0.006	0.05	—	0.15
A₂	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	—	0.008	0.09	—	0.20
D	—	0.393	—	—	10.00	—
E	—	0.393	—	—	10.00	—
e	—	0.020	—	—	0.50	—
H_D	—	0.472	—	—	12.00	—
H_E	—	0.472	—	—	12.00	—
L	0.018	0.024	0.030	0.45	0.60	0.75
L₁	—	0.039	—	—	1.00	—
y	—	0.004	—	—	0.10	—
θ	0	3.5	7	0	3.5	7

28.3 48L LQFP (7x7x1.4mm footprint 2.0mm)



29 REVISION HISTORY

REVISION	DATE	PAGE	DESCRIPTION
V0.1	2011/8/30		Preliminary release.
V0.2	2012/03/20		1. Remove MT510 part 2. Update the package and pin assignment.
V0.3	2012/10/12		1. Update the part numbers with MT510, MT520 and MT530. 2. Update the pin assignment and description 3. Update the general purpose I/O 4. Update the timer/counter 5. Update the basic PWM function 6. Update the enhance PWM function 7. Update the analog comparator function
V0.4.	2014/04/09		1. Change part name from MT5xx to NM15xx.
V0.5	2014/06/19		1. Update the Parts List in chapter 4.
V0.6	2014/7/18		1. Update the Specification of 12-bit SARADC
V0.7	2014/7/25		1. Correct P7.4 and P7.5 about comparator input in Pin Description.
V0.8	2015/2/25		1. Correct the content of LDROM size in chapter 2.
V0.9	2016/03/01		1. Correct pin assignment of IC10~IC12. Modify chapter4 of part list, chapter5 of pin configuration
V0.9.3	2017/05/22		1. Add new part of NM1521 LQFP64

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